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Power Efficient Implementation of Low Noise CMOS LC VCO using 32nm Technology for RF Applications

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Abstract—

Voltage Controlled Oscillator (VCO) is an integral component of most of the receivers such as GSM, GPS etc. As name indicates, oscillation is controlled by varying the voltage at the capacitor of LC tank. By varying the voltage, VCO can generate variable frequency of oscillation. Different VCO Parameters are contrasted on the basis of phase noise, tuning range, power consumption and FOM. Out of these phase noise is dependent on quality factor, power consumption, oscillation frequency and current. So, design of LC VCO at low power, low phase noise can be obtained with low bias current at low voltage. Nanosize transistors are also contributes towards low phase noise. This paper demonstrates the design of low phase noise LC VCO with 4.89 GHz tuning range from 7.33-11.22 GHz with center frequency at 7 GHz. The design uses 32nm technology with tuning voltage of 0-1.2 V. A very effective Phase noise of -114 dBc / Hz is obtained with FOM of -181 dBc/Hz. The proposed work has been compared with five peer LC VCO designs working at higher feature sizes and outcome of this performance comparison dictates that the proposed work working at better 32 nm technology outperformed amongst others in terms of achieving low Tuning voltage and moderate FoM, overshadowed by a little expense of power dissipation.

Keywords— Voltage Controlled Oscillator, Phase Locked Loop, Low Power, Low Noise

I. INTRODUCTION

The voltage controlled oscillator is characterized by alteration of its frequency available at its output according to the input variation of voltage [1]. Control voltage input to VCO can be modulated to incur Frequency Modulation (FM) or Phase Modulation (PM) [2][3]; Control voltage input to oscillator is converted into current first and then current is converted into frequency[1]. High performance monolithic VCO design is upfront research area in the modern times [4-5]. A CMOS VCO is in general constituted by ring topology, LC tuned circuit or relaxation circuits [2]. The equation (1) shows the basic definition of VCO.

$$\Omega_{out} = \omega_0 + K_{vco} * V_{control} \quad (1)$$

Here, ω_0 symbolizes the intercept corresponding to $V_{control} = 0$ and K_{vco} indicates the 'gain' and 'sensitivity' of the circuit [2]. The phase noise and Figure of merit (FOM) concerning LC VCO are explained below:

A. *Phase Noise*

The phase noise in the oscillator has great importance because poor phase noise can lead to the degradation in the performance of the whole transceiver. Oscillator consists of active and passive devices. Noise sources can be divided into two groups, namely device noise and interference. All devices exhibit some noise such as flicker noise, thermal noise and shot noise, which lies in the category of device noise. Therefore, the substrate noise lies in the later group. Phase noise is the random variation of the frequency signal from its actual position or from its ideal position. The phase noise in actual oscillator cannot be removed totally and there is no phase noise in an ideal oscillator. In RF circuits, the phase noise means that the output signal contains the energy components at other frequencies rather than from its carrier signal frequency. The spectrum in actual oscillator shows some skirts around the carrier signal while the spectrum of ideal oscillator shows shape of an impulse. The phase noise is expressed as unit bandwidth at an offset frequency(Fig. 1) of $\Delta\omega$ with respect to $\omega 0$ or it can also be expressed as ratio of power at particular offset frequency $\Delta\omega$ from the carrier to the power at center frequency. The unit of phase noise is "dBc/Hz". The phase noise can be expressed by equation,

$$L(\Delta\omega) = 10 \log \left(\frac{P_{1Hz}(\omega_o + \Delta\omega)}{P_c} \right)$$

where Pc is the carrier power and ω_0 represents the carrier frequency. The above expression shows that phase noise can be improved significantly as Pc is increased.

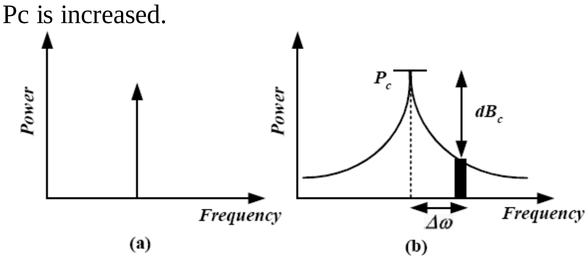

Fig. 1 Frequency spectrum of an (a) Ideal (b) practical

B. Figure of Merit (FOM)

The figure of merit (FOM) is one of the key factors which is most widely used to examine the performance of the oscillator. The phase noise, power dissipation, offset frequency and carrier frequency are used in the formulation. The designers use this formulation to compare their oscillator performance with the state of the art work. Low phase noise at higher frequencies is one of the key challenges which are observed with FOM. The FOM can be given by Eq.

$$FOM = L(\Delta\omega) + 20\log\left(\frac{\omega_o}{\Delta\omega}\right) - 10\log\left(\frac{P_{diss}}{1mW}\right)$$

Throughout where P_{diss} is the dc power dissipated in the oscillator and L ($\Delta\omega$) is the phase noise equation used in this paper to calculate FOM.

II. LITERATURE SURVEY

Ching-Yuan Yang and his friends [6] employed a tunable inductor in the VCO making use of a transformer to compensate for the energy loss. The the tuning frequency and low noise of the output signals is getting facilitated by VCO, along with a variable inductor which suits both criteria. A small-area stacked transformer is used in the 7-GHz VCO, which attains a tuning range of 6.59 to 7.02 GHz and measured phase noise of −114 dBc/Hz at 1-MHz offset from a 6.59-GHz carrier while consuming 9 mW from a 1.2-V supply.

Abhishek Agrawal [7] designed CMOS LC VCO with Octave Frequency Tuning-range for wideband radios. An area and power-efficient resonant mode-switching approach is presented that enables wide-FTR oscillators without compromising inductor Q, resulting in low phase noise and high VCO Figure-of-Merit (FoM).

Davood Fathi [8] designed an NMOS only cross-coupled LC-tank VCO that imbibes an extra symmetric centre tapped inductor between the source ends of the cross-coupled transistors. This inductor leads to an improvement of the phase noise of VCO about 3.5 dB. At 0.46 V supply voltage, the output phase noise is −107.8 dBc/Hz at 1 MHz offset frequency from the carrier frequency of 10.53 GHz. The resulting DC power consumption is limited to 0.346 mW.

Lytrosyngounis and T. Noulis [9] designates a high speed cross-coupled LC Voltage Controlled Oscillators in which phase noise analysis is done at 1-GHz, 10-GHz and 20-GHz carrier frequency operation, designed in a 65nm CMOS process, commercially available by TSMC. Detailed noise simulation analysis is carried out with respect to phase noise performance optimization in all three VCOs, setting specific comparison constraints such as keeping identical transistor sizing and bias settings while only modifying the passive LC tank.

Sameh Soliman [10] used new tuning technique to tune its output frequency. Simulation results shows that it provides quadrature and differential outputs; operates with 10-GHz center frequency,600-MHz tuning range centered around its center frequency, and phase noise of -95dBc/Hz at I-MHz offset from the fundamental harmonic of its output; and draws 10rnA of DC current from a single, 1.8-V power supply.

III. DESIGN

The design was simulated on Tanner Tool and Advanced Design System using 32nm technology.

Figure 2 shows the schematic of LC VCO which is working at 1.2 V supply with power consumption of 8.29 mW. This VCO is generating oscillation between 7.33-12.22 GHz with tuning range of 4.89 GHz.

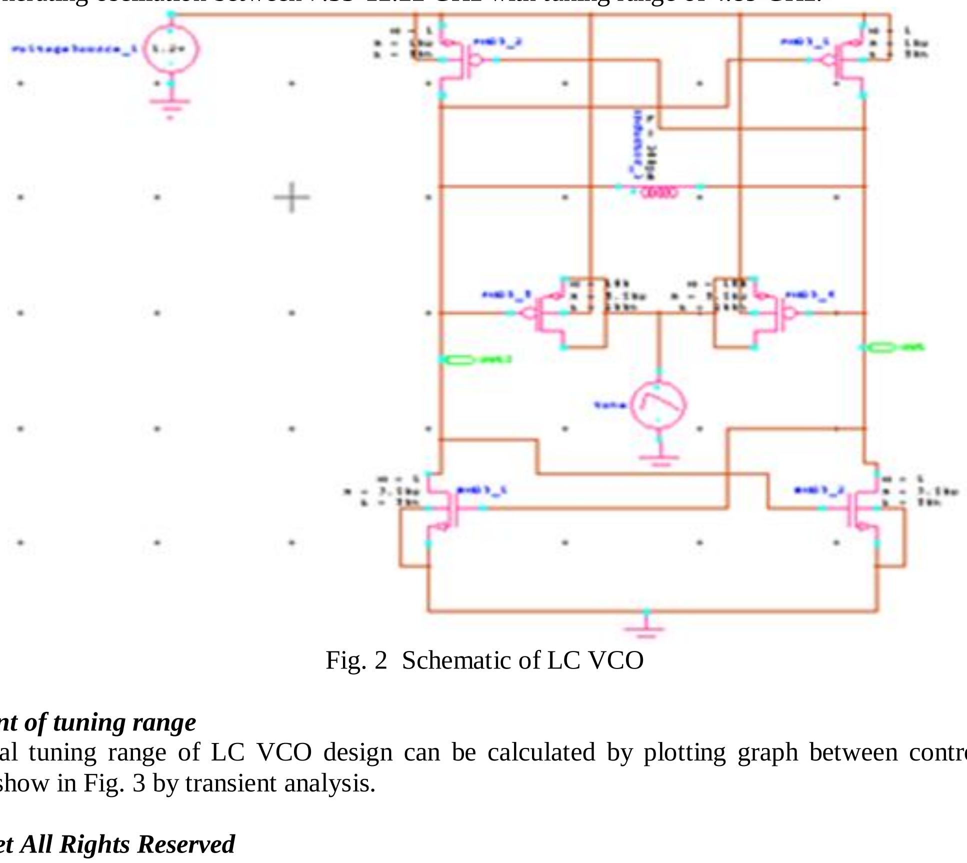

Fig. 2 Schematic of LC VCO

A. Measurement of tuning range

The fractional tuning range of LC VCO design can be calculated by plotting graph between control voltages and frequencies as show in Fig. 3 by transient analysis.

$$Fractional\ Tuning\ Range = \frac{f_{max} - f_{min}}{f_0} \times 100$$

By the graph is clear that f_{max} and f_{min} is 12.22GHz and 7.33 GHz where f_0 is 7 GHz.

B. Power Consumption

The power consumption of VCO can be calculated by formula given below:

$$\text{Max D.C. power dissipation} = V_{supply}\ I_{bias}$$

It gives total power consumed by the integrated parts in the circuit. The power consumed by this VCO is 8.29 mW.

IV. RESULTS

A. Tabulation of Parameters extracted

Table I : Results of CMOS LC VCO

S. No.	Parameter	Simulation result
1.	Technology	32nm
2.	Power Consumption(mW)	8.29
3.	Frequency(GHz)	7.33-12.22
4.	Tuning Voltage(V)	0.0-1.2
5.	Phase Noise(dBc/Hz)	-115@1MHz
6.	FOM(dBc/Hz)	-183

B. Phase Noise and FOM

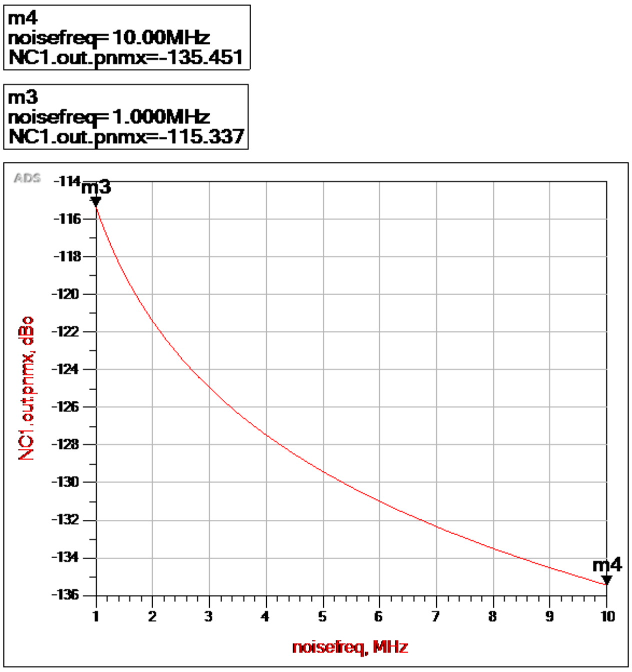

Fig. 3 shows that the phase noise at an offset of 1MHz and 10 MHz is -115 dBc/Hz and -135 dBc/Hz at 7.33 GHz-12.22 GHz.FOM of the proposed VCO is -183 dBc/Hz at 1MHz offset.

C. Frequency versus tuning voltage

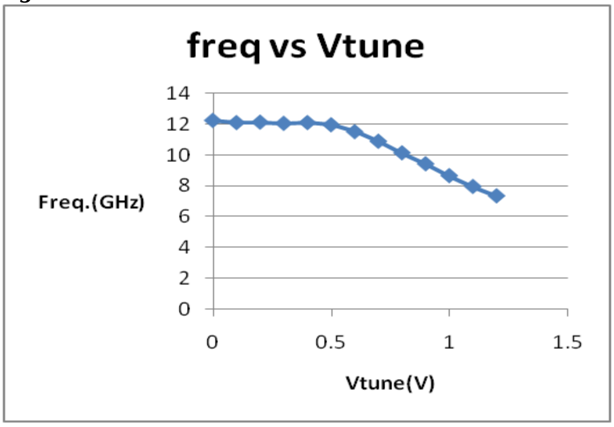

Fig.4 Frequency versus tuning voltage graph

D. Waveform

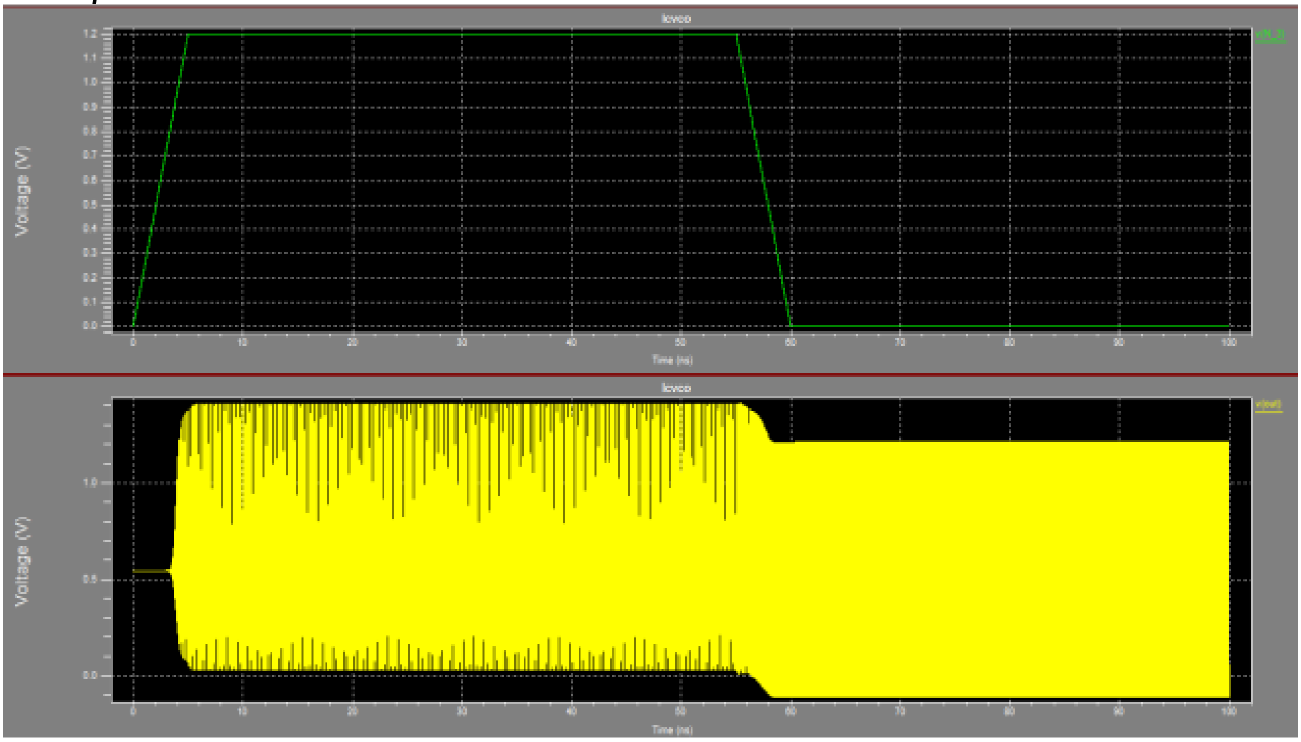

Fig.5 Frequency from 7.33-12.22 GHz with input from 0-1.2 V

Fig. 5 shows the waveform with tuning voltage of 0-1.2 V. While input is 1.2 V, the VCO is generating oscillation of 12.22 GHz and when input is 0V, then VCO is generating 7.33 GHz. Tuning range in frequency is of 4.89 GHz.

V. COMPARATIVE STUDY OF RESULTS

Table III : Performance Comparison of LC VCOs

S. No.	Parameter	Ref. [6]	Ref. [7]	Ref. [8]	Ref. [9]	Ref.[10]	Proposed work
1.	Technology (nm)	180	65	180	65	180	**32**
2.	Supply Voltage (V)	1.2	0.6	0.46	0.95	1.8	**1.2**
3.	Power Consumption(mW)	6.36	10	0.346	3.6	18	**8.29**
4.	Frequency (GHz)	6.59-7.02	6.39-14	10.53-11.35	10	10-10.6	**7.33-12.22**
5.	Tuning Voltage(V)	0-1.2	-	0-1.8	-	0.6-1.8	**0-1.2**
6.	Tuning Range(GHz)	0.43	7.61	0.82	-	0.6	**4.89**
7.	Phase Noise(dBc/Hz)	-104/1MHz	-112/1MHz	-107.8/1MHz	-102/1MHz	-95/1MHz	**-115@1 MHz**
8.	FOM(dBc/Hz)	-172.9	-186	-193.8	-	-	**-183**

VI. CONCLUSION

Low power, low phase noise LC VCO has been designed in this research work keeping in view nanotechnology paradigm working at 32 nm technology. Since phase noise is dependent on many parameters, so out of those, state of the art technology working out in the industry, 32 nm is chosen to show the impact of nanotechnology on phase noise. This VCO exhibits low power of 8.29 mW with supply of 1.2 V. Phase noise of -115 dBc/Hz is obtained using basic LC VCO architecture with tuning range of 4.89 GHz and oscillation frequency of 7.33-12.22 GHz.

REFERENCES

[1] B. Razavi, A Study of phase noise in CMOS oscillators, IEEE ;J. Solid- State Circuits, vol. 31, No. 3 (March 1996).

[2] B. Razavi, Design of analog CMOS integrated circuits, Tata McGraw Hill Edition 2002.

[3] Shailesh S. Rai and Brian P. Otis, A 600 _ W BAW – Tuned Quadrature VCO Using Source Degenerated Coupling, IEEE Journal of solid-State Circuits , Vol. 43, No.1, (January 2008).

[4] Babak Soltanian, Herschel Ainspan, Woogeun Rhee, Daniel Friedman, and Peter R. kinget, An Ultra-Compact Differentially Tuned6-GHz CMOS LC-VCO With Dynamic Common-Mode Feedback IEEE Journal of solid-State Circuits , Vol. 42, No. 8, (August 2007).

[5] T.H. Lee and J.F. Bulzacchelli, A 155-MHz Clock recovery delay-and Phase-Locked Loop, IEEE J. Solid-State Circuits, Vol. 27, No.12, (December 1992).

[6] Ching-Yuan Yang, Meng-Ting Tsai, High Frequency Low Noise Voltage Controlled LC-Tank Oscillators using Tunable Indcutor Technique,IEICE Trans.Electron.,Vol.E89-C,No.11 November 2006.
[7] Abhishek Agrawal, Arun Natarajan, A 6.39GHz-14GHz Series Resonator Mode-Switching Oscillator with 186-188dB FoM and 197dB FoMA in 65nm CMOS,IEEE Radio Frequency Integrated Circuits Symposium,2015.
[8] Davood Fathi, Aboozar Gorbani Nejad, Ultra-Low Power, Low Phase Noise 10 GHz LC VCO in the Subthreshold Regime, Circuits and Systems, 2013, 4.
[9] C. Lytrosyngounis ,T. Noulis, Phase Noise Performance Analysis of High Speed Cross Coupled CMOS LC VCOs, IEEE International Conference on Modern Circuits and Systems Technologies, 2016.
[10] Sameh Soliman, 10-GHz wide tuning-range linear voltagecontrolled Oscillator, Theses and dissertations, 2003.