International Journal of Emerging Research in Management &Technology
ISSN: 2278-9359 (Volume-6, Issue-4)

Research Article | **April 2017**

Low-Power High Speed 1-bit Full Adder Circuit Design in DSM Technology

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Abstract—

As the number of transistors per die have increased with the advancement/ development in the CMOS technology and the need of greater performance have become the primary driving factor in semiconductor industry. As more number of transistors can be integrated into a single package, more and more components of systems can be packaged into a single chip. This has not just reduced the size of the chip but also cost and delay to a great extent. The GDI cell is similar to a CMOS inverter structure. In a CMOS inverter, the supply voltage (V_{dd}) and the ground voltage (V_{ss}) are connected to the source of the PMOS and NMOS respectively whereas in a GDI cell it is not necessary to connect supply and ground voltage with MOS diffusions. In such designs of hybrid GDI gates, pass transistors are activated only in cases where threshold drop occurs at the output. In this paper comparison of all conventional static CMOS technique like 28T, SERF, 8T, 6T and GDI technique with swing restoration buffers with proposed circuit Propagation delay of Hybrid GDI based OR gate is less than CMOS but more in AND and XOR. Hence the total power delay product (PDP) value is also less only in OR gate. All the simulation is performed in Cadence Virtuoso at 180nm and 65nm technology at 100MHz, 200MHz and 1GHz.

Keywords— GDI, Full Adder, XOR, XNOR, Low power

I. INTRODUCTION

As the number of transistors per die have increased with the advancement/ development in the CMOS technology and the need of greater performance have become the primary driving factor in semiconductor industry. As more number of transistors can be integrated into a single package, more and more components of systems can be packaged into a single chip. This has not just reduced the size of the chip but also cost and delay to a great extent. Due to increased competition in the semiconductor industry, chip manufacturer are chasing these goals aggressively [1-2]. The increased in number of transistors per die is increasing exponentially. But in this process power dissipation in the integrated circuit (IC) is also growing. So in the present scenario, the reduction of excessive power consumption in the circuit has become a dominant concern. Higher power consumption leads to shortened battery life and also increased on-chip temperatures, which may reduce the operating life of the IC. For portable electronics, longer battery life is one of the important design constraints. Hence for portable electronics low power consumption is a crucial requirement. However power consumption is not only issues in portable electronics but also IC's that consume more power dissipate more heat and hence more expensive cooling systems are needed to sink the excessive heat. So if the power reduced even to a small extent can reduce the use of such expensive cooling devices and in the consumer market can leads to a significant profits. Thus we can say that heat dissipation and excessive cooling reduction directly impact the cost of an IC [3].

Hence low power consumption has become zero order constraints and high performance per-watt has become a new task for microprocessor chip manufactures today.

The power consumption of the circuit can calculate.

$$P_{avg/gate} = P_{leakage} + P_{switching} + P_{short\ circuit} \qquad (1.1)$$

Where $P_{leakage}$ is the power consumed when we scale the channel length in nanometer regime it increases with temperature of the circuit increases in ideal state. $P_{switching}$it occurred due to charging and discharging of pull up and pull down network. $P_{short\ circuit}$ occurred due to charging and discharging of internal capacitances of the transistor from V_{dd} to Gnd.

Recently, the GDI (Gate Diffusion Input) technique is emerged as a promising alternative to Standard CMOS Logic [4]. The GDI technique has reduced power dissipation and less delay with least number of transistor counts in design of any digital system. Similar to other existing techniques, GDI also suffers from low output swing voltage problem due to low threshold voltage [5]. This research work tried to overwhelm this problem by adding an additional pass transistor to GDI cell. Implementations of proposed method in few digital circuits provide better result in terms of power reduction and delay.

The conventional CMOS one bit digital signal adder cell is shown in Figure.2.8. The size of each transistor is taken from [5-7]. The CMOS structure of adder cell is taken because of the regularity of design and it consists of 28 transistors in the design. Different logic styles can be investigated from different points of view. But they tend to favor one performance aspect at the expense of others[19-20]. In other words, it is different design constraints imposed by the

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application that each logic style has its place in the cell library development. Even a selected style appropriate for a specific function may not be suitable for another one[8-15].

II. LITERATURE SURVEY

In our literature survey, different abstraction levels for power optimization in CMOS circuits are studied. Also the three main components responsible for power dissipation are studied and the different techniques/ methods used to minimize these components in various research papers are reviewed. In this research we also surveyed the different transistor level techniques used to design low power CMOS digital circuits. Several research have been done in this area in last decades and we found that the recently proposed GDI technique is emerging as promising alternative of CMOS logic style for low power design with less number of transistors [9-11].

In digital circuit design. Survey includes the different power optimization methods at various level of digital circuit design process from system level to physical level. Different sources responsible for power dissipation in CMOS circuits are also reviewed. Techniques to reduce the effect of such sources in different research articles are discussed here.

ArkadiyMorgenshteinet. al.,2009, presented a new technique for low-power digital combinatorial circuit design called Gate Diffusion Input technique. Basic GDI technique suffers from low threshold voltage that degrades the performance of digital circuits. Problem of low swing threshold voltage drop in GDI is discussed and how it is removed in proposed Hybrid GDI technique is explained.

Thedetailed analysis of GDI/ Hybrid GDI technique- its cell structure design, operational and transient analysis, switching characteristics, fan-in and fan-out bounds, swing restoring buffer analysis are discussed.An 8-bit CLA adder was fabricated using GDI and CMOS. Simulation result shows 45% reduction of power-delay product in the test chip in GDI over CMOS and significant improvements in performance, as well as decreased number of transistors and area in most simulated GDI circuits over CMOS and PTL.

Adarsh Kumar Agrawalet. al.,2009, presented a design of full adder using Mixed Gate Diffusion Inputstopology based on static CMOS inverter. For this, in the long chain of full adders, the GDI full adders are followed by inverters to improve the performances with respect to conventional single full adder chain. The propagation delay, dynamic and leakage power dissipation can be optimized by changing the number of full adders between two consecutive inverters.

HSPICE simulation using TSMC 0.35µm and 0.18µm CMOS technologies evaluated propagation delay and average power for minimum power design. Their proposed circuit is 18 to 48% and 7 to 26% faster than the previous circuits at 0.35µm and 0.18µm CMOS technologies respectively. Subsequently the average dynamic power of their proposed circuits is 8 to 12% and 14% to 28% lower than the previous circuits at 0.35µm and 0.18µm CMOS technologies respectively.

Initially GDI is proposed for SOI and twin well technology, later, *ArkadiyMorgenshteinet. al.,2010,* proposed CMOS compatible GDI design technique in which the bulks of pMOS and nMOS transistors are constantly connected to supply and ground respectively. Simulations of basic GDI gates under process and temperature corners in 40nm CMOS achieves 70% leakage and 50% active power reduction while having the same delay as compared to CMOS.

VahidForoutanet. al.,2014, presented two new symmetric designs for low- power, high speed full adder cells using GDI structure and hybrid CMOS logic style. The ULPD (Ultra Low- Power Diode) logic-level restorer is used in adders for full-voltage swing. The circuits are optimized for energy efficiency at 0.13 µm and 90 nm partially depleted (PD) SOI CMOS process technology. Simulations performed on HSPICE and the comparison with standard full adder cells shows excessive improvement in terms of Power, Area, Delay and Power-Delay-Product (PDP).

A digital signal full adder cell produces a two-bit output which is carry and Sum .Full Adder cell is implemented in low power and high performance data path circuit and complex communication systems. The full adder consist of three input signals, i.e., A, B, and C (carry in), and two output signals sum and carryout which is shown in Fig.1.

The basic operation of full adder is given by the standard Boolean expressions as,

$$CARRY = AB + BC + CA$$

$$SUM = ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C}$$

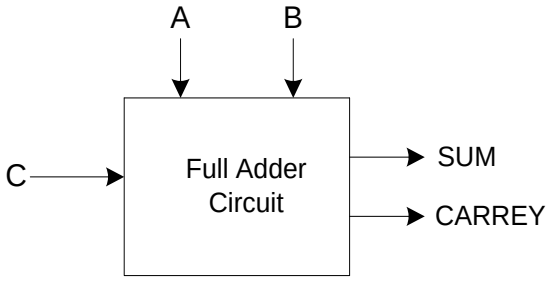

Fig.1 Basic Full Adder Circuit.

Gate Diffusion Input (GDI) technique to improve output swing voltage level of circuits and is named as Hybrid GDI technique. The GDI technique is first introduced by Arkadiy Morgenshtein in 2002 [4] for fabrication in twin well CMOS process or Silicon on Insulator (SOI) technology. Later in 2010, he proposed its compatible version to implement in standard CMOS process [5]. Table I. shows the Logic Faction Values with the proposed technique. The GDI technique is introducing as the promising alternative to static CMOS logic.

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Table I: Logic Faction Implementation with GDI Technique

N	P	G	Out	Function
0	B	A	$\overline{A}$.B	F1
B	1	A	$\overline{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}$B+AC	MUX
0	1	A	$\overline{A}$	NOT

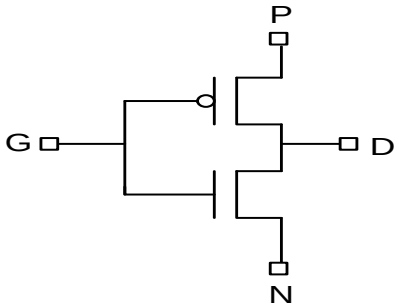

Fig. 2: Symbol of GDI cell

This technique shows great reduced in power dissipation and propagation delay using few numbers of transistors to implement any digital circuit. This chapter explains methodology of basic GDI and Hybrid GDI for digital circuit design as shown in Fig.2.

The GDI cells can also successfully implemented for designing low power combinational circuits using special properties of combinational logic pre-computation and Shannon expansion. The property of pre-computation means the transitions of logic values are prevented from propagating through the circuit if the final result does not change with these transitions [15].

Static Energy Recovery Full Adder (SERF)

As an initial step toward designing low power arithmetic circuit modules, we designed a Static Energy Recovery Full adder (SERF) cell module. The cell uses only 10 transistors and it does not need inverted inputs. The design was inspired by the XNOR gate full adder design [10]. It should be noted that the new SERF adder has no direct path to the ground as shown in Fig.3. The elimination of a path to the ground reduces power consumption, removing the Psc variable (product of Isc and voltage) from the total power . The charge stored at the load capacitance is reapplied to the control gates [11]. The combination of not having a direct path to ground and the re-application of the load charge to the control gate makes the energy recovering full adder an energy efficient design.

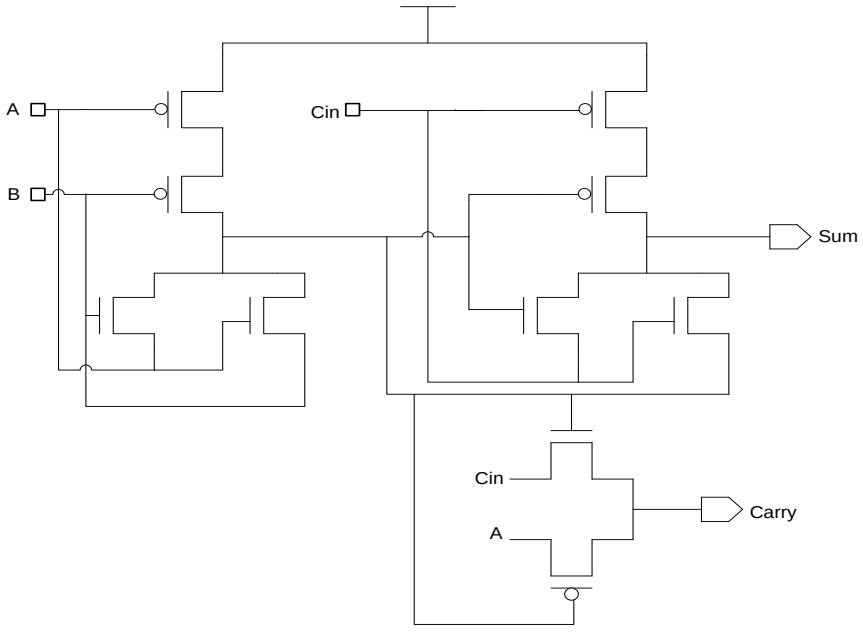

Fig.3: Schematic of SERF Full Adder

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8 T Full Adder Circuit

The basic of 8T full adder consists of 3 modules: 2 XOR elements and a Carry. The Sum output is obtained by two XOR blocks in succession. For the carry section GDI based 2TMUX is used and (A XOR B) as the selection signal. The Sum and the C_{out} module need 6 and 2 transistors respectively [11]. The transistor level implementation of the eight transistor full adder. It is obvious from the figure that both SUM and C_{out} has a maximum delay of 2T. It doesn't suffer from threshold voltage loss problem. Also the noise margin has been substantially increased by proper sizing of transistors in 3T XOR. The power delay product (PDP), and the area of the proposed adder are also found better than that of the existing.

HYBRID GDI AND GATE

The AND gate is a basic digital logic gate that implements logical conjunction. It behaves according to the truth table shown in Table II. Its output is HIGH if all the inputs are at high logic state and output is LOW if any one input is low. In other words, AND gate finds the minimum between two binary numbers. Hence, the output of AND gate is always zero except the condition when all inputs are one [17].

Table II: Truth Table of AND gate

INPUT		**OUTPUT**
A	**B**	**A AND B**
0	0	0
0	1	0
1	0	0
1	1	1

Design of AND gate based on GDI technique using two transistors where source of pMOS is connected to ground and source of nMOS is connected to second input B. The output voltage level for different input combinations of GDI AND gate. To compatible with standard CMOS process, the bulk of pMOS and nMOS of GDI cell are connected to supply and ground respectively [18-20].

III. PROPOSED WORK

In proposed Hybrid GDI based design of XOR gate, the effect of threshold voltage drop is tried to remove by adding one more GDI cell controlled by inverted gate input of main GDI. In over proposed circuit we have generated XOR and XNOR operation with the help of three transistor (3T), when XOR pass through inverter it generate XNOR operation. Intermediate XOR and XNOR are generated using three transistor (3T) XOR and XNOR gate. Sum and Carry are generated using two double transistors multiplexers. 3T XOR and XNOR consume high energy due to short circuit current in ratio logic. They all have double threshold losses in full adder output terminals which usually prevents the full adder circuit from operating at low supply voltage or in cascade directly any without extra buffers. The lowest possible power supply is limited to 2Vtn + Vtp where Vtn and Vtp are the threshold voltages of nMOS and pMOS respectively. The basic advantages of 13T transistor full adders are: less area compared to higher gate count full adders, lower power consumption and lower operating voltage.

In Hybrid GDI based XOR gate, one more GDI cell has been added which is controlled by inverted input gate signal of first GDI cell. When A = 0, pMOS of GDI cell 1 and nMOS of GDI cell 2 conducts simultaneously. When B = 0, GDI cell 2 acts as an inverter and provides inverted input signal A at output end. It means, for B = 0, A = 0, XOR out is '1' and for B = 0, A = 1, XOR out is '0'. Similarly when B = 1, GDI cell 1 act as an inverter and for B = 1, A = 0, XOR out is '1' (V_{dd}) and for B= 1, A = 1, XOR out is '0'.

Similarly, other gates and gates with more inputs can be designed using proposed Hybrid GDI technique. This research work implemented few most common digital circuits using conventional CMOS technique, basic GDI technique with buffer insertion for full swing and Hybrid GDI technique. Circuits are simulated and their comparative performances are analysed. The XOR (Exclusive-OR) gate is a digital logic gate which has a HIGH output if inputs are different and output is LOW if inputs are same either zeros or ones. The function of XOR gate is to find inequality between two binary numbers. In other words, XOR gate says 'one or the other but not both'. Truth table of XOR gate is shown in Table III.

Table III: Truth Table of XOR gate

INPUT		**OUTPUT**
A	**B**	**A XOR B**
0	0	0
0	1	1
1	0	1
1	1	0

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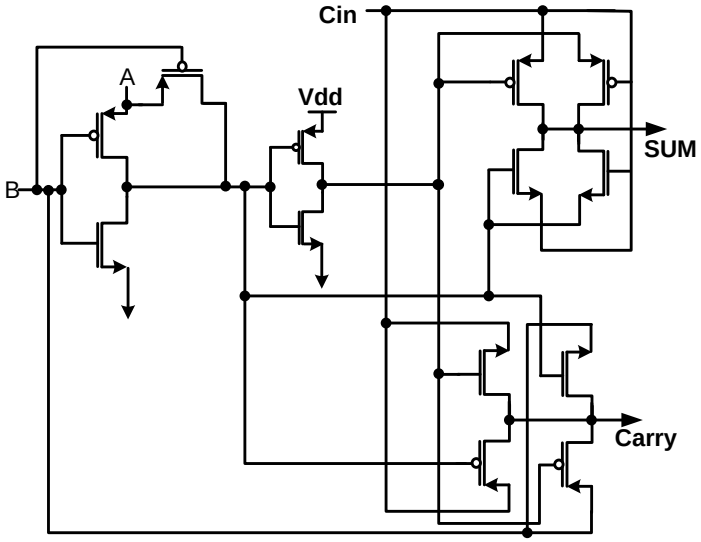

Fig. 4: Proposed 13T Hybrid GDI Adder Circuit

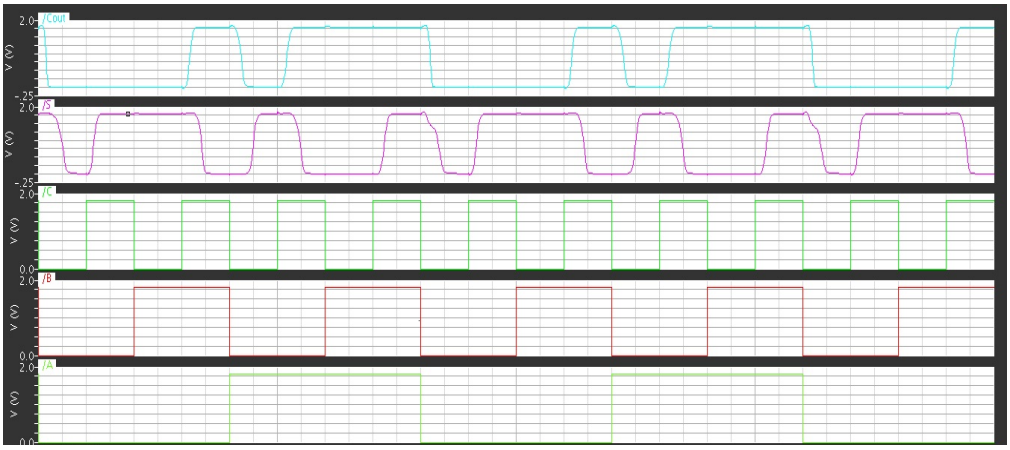

Fig. 5: Output Waveform of Proposed Circuit

IV. SIMULATION RESULTS AND DISCUSSION

All the existing and proposed circuit is simulated in Cadence Virtuoso at 180nm technology with supply voltage of 1.8V. Power consumption is calculated with the variation of frequency at lower frequency (10MHz), middle frequency (200MHz) and high frequency (1GHz). We obsrve that as we increase the frequency the power consumption of the adder circuit also increases as shown in Fig.4 and Fig.5. The size (W/L ratio) of the transistors (N-CMOS and P-CMOS, respectively) is set to be the same, so that the comparison of power dissipation between different types of adder circuits is distinct. In our work, the clock frequency changes from 10 MHz to 1 GHz to investigate its influence on power dissipation of different types of adder circuits. the proposed adder shows 51.5% reduction in power 93.3% reduction in delay and 96.8% reduction in PDP at 10MHz frequency with reference to conventional CMOS .

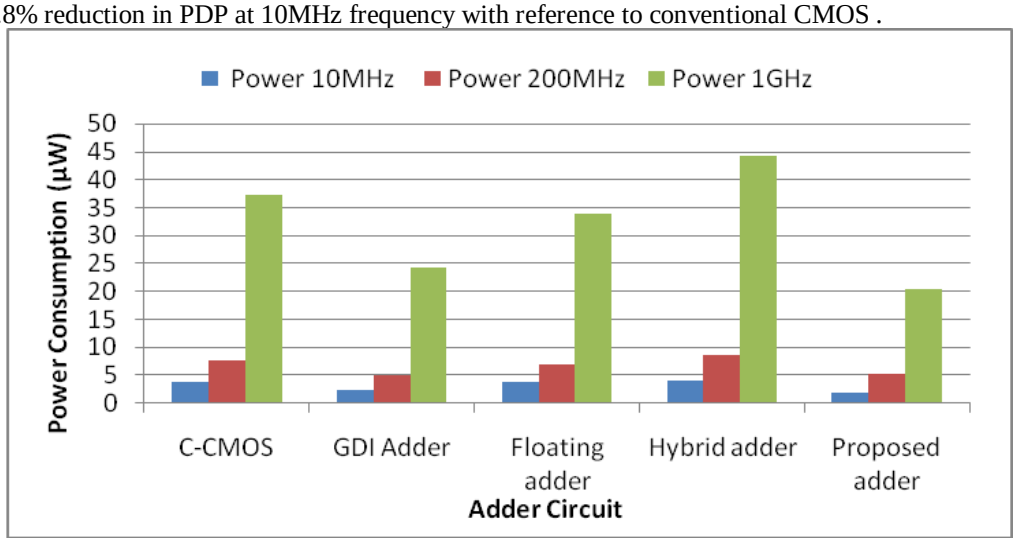

Fig.6: Comparison of Power consumption of existing and Proposed Adder Circuit

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V. CONCLUSION

In this research, an efficient methodology is presented to improve the output swing level of GDI gates. New designs of GDI based basic digital (AND, OR, XOR) gates are presented using single pass transistors to improve swing level of GDI gates. The new design of basic gates with combination of GDI logic and pass transistor logic is called hybrid GDI technique. In such designs of hybrid GDI gates, pass transistors are activated only in cases where threshold drop occurs at the output. The proposed GDI is the modification in basic GDI gates by adding single swing restoring pass transistor. The proposed Hybrid GDI is the modification in basic GDI gates by adding single swing restoring pass transistor. With Hybrid GDI technique, the circuit energies are conserved rather than dissipated as heat. Besides the power reduction, Hybrid GDI technique also provides reduction in delay and size as compared to conventional CMOS technique.

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