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Critical Component Identification in Analog Electronic Circuits using Sensitivity Analysis

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Abstract—

Fault diagnosis of Analog Electronic circuits involves an exhaustive analysis of each and every component of the circuit. This is a procedure which is an analysis of each and every component and the complexity increases as the number of components increase. The faults in different components have varied effects on the performance of the circuit and some of the components are more critical than others. In this paper a method has been proposed to identify the critical components in an Analog circuit being diagnosed for faults. Sensitivity Analysis is used to identify these critical components. A second order Butterworth Filter is used to illustrate the method proposed in this paper. In this paper an algorithm has been proposed which identifies the most critical component of the circuit.

Keywords— Critical Components, Sensitivity Analysis, Cut off frequency, Multi Frequency approach.

I. INTRODUCTION

Fault diagnosis of electronic circuits is of immense research interest for the past few decades. Analog circuits are used in many electronic systems such as home electronics, automotive electronics, industrial electronics, defence electronics, mobile electronics etc. The diagnosis of digital electronic circuits is well established, documented and implemented. The diagnosis of digital circuits is relatively less complicated when compared to the fault diagnosis of analog electronic circuits. The fault diagnosis of analog circuits is complex as it involves infinite number of combination of faults like tolerance of the component values. Also in most of the cases full knowledge of the circuit is not known and this creates a black box type of situation. The analog testing now has to be expedited by including Built in Self Test (BIST) and Design for Testability (DFT) by making them part of the design cycle of the IC fabrication process [1]. In this digital world most of the analog functions are translated into their digital equivalents, but significantly chips need the incorporation of analog circuits also [2].

The most popular methods of fault diagnosis is Simulation Before Test (SBT) approach and Simulation after Test (SAT) approach. In this paper the method used is SBT approach. In SBT approach the circuit under test (CUT) is simulated for all possible faults first and then the results are tabulated in a table called Fault Dictionary Table. The Fault Dictionary Table is constructed using methods like multi frequency method, multi nodal method etc. The size of the Fault dictionary is directly proportional to the number of faults being tested and generally becomes huge when the number of faults being diagnosed is high. Several optimization techniques are used to reduce the size of the dictionary thus taking finite time to diagnose faults.

II. ANALOG FAULT DIAGNOSIS – SENSITIVITY

The main challenges today in analog fault diagnosis are to design universally accepted fault models, cost effective, faster and accurate diagnosis of faults. Importantly all this is desired even in the presence of inherent characteristics of analog circuits like tolerances, non linearity and in- accessible test nodes etc. A method to locally diagnose the non-linear dc circuits has been proposed. The fault diagnosis has been carried out by the rank test matrix based on input-output models [3]. Anil Pahwa and Ronald A. Rohrer [4] used band faults to construct fault dictionaries. Nodal analysis has been used to illustrate the ideas of both the Band faults and fault bands. Fault band is an exact approach, it first finds the non linear response when a catastrophic fault occurs and then does worst case analysis. Band fault method first finds the nominal worst case boundaries and then the faults are separated. An algorithm is proposed based on Simulation after test approach [5]. T.N. Trick and Y.Li proposed a new first order sensitivity fault isolation algorithm [6]. The independence of the sensitivity vectors indicates that the test points are capable of identifying faults. The degree of the testability of the circuit under test is determined by the rank of the sensitivity matrix of the columns. In this paper a method is proposed where the size of the ambiguity group is reduced by considering only the positive real parameter values. Hierarchical symbolic analysis methods are being developed in a big way in the recent years and are very useful to fault diagnosis of the linear analog circuits. These are used effectively to reduce the huge amount of time taken in sensitivity and tolerance analysis [7]. A graph based algorithm is used to select test points and stimuli automatically [8]. The criterion in selecting test points is maximum fault isolation. The selection of test stimuli uses sensitivity matrix. This method is cost effective as it does not use expensive circuit simulations. The residual generation is done by using robust detection filters and thresholds. The thresholds are important as they decide the effect of noise on

the fault isolation system. Proper design of threshold levels reduces the noise effects on the system. A modified version of the method using large change sensitivity for D.C. non linear circuits fault simulation is presented [9]. Symbolic analysis is used in the calculation of the column rank of the sensitivity matrix [10]. As symbolic analysis can handle only small circuits, DDD which is a graph based approach is used to deal with larger circuits. A combination of methods based on sensitivity, information channel and an integer coded dictionary formulation is used to diagnose faults [11]. The sensitivity based method is used to find ambiguity sets, the information channel based method is used to find the minimum set of measurements and the integer-code dictionary is based on the quasi Hamming distance. Also the efficiency of the technique is compared with a method based on entropy index. Test frequencies are selected using algebraic indices of a sensitivity matrix [12]. The matrix is obtained from the testability analysis of the circuit. Using test index (TI) selection of test frequencies is made which isolate maximum number of parametric faults. Sensitivity analysis and fuzzy logic have been used to analyze tolerance effects. The sub circuit extraction problem is similar to sub graph isomorphism. Fuzzy attributed graphs are used in sub graph isomorphism [13]. J.A. Starzyk and D. Liu [14] used ideal switches to indicate stuck-at, bridging and stuck-open faults. The resulting circuit is then analyzed to identify the stuck faults. The SBT approach has been used to develop an automatic system to select frequencies has been proposed. The measured values are compared with the set of examples in the fault dictionary. Global sensitivity analysis method and fuzzy processing method are applied to obtain sensitivity curves. Fang Liu and others [15] used Bayesian frame work to diagnose parametric faults in circuits. As this method requires lots of statistical profiling, a hierarchical process variability analysis is used. Sensitivity analysis has been used to select measurement data which will isolate maximum faults.

III. CRITICAL COMPONENTS

In this paper critical components are identified in an analog electronic circuit by using sensitivity analysis. The method proposed in this paper has several advantages and helps in reducing the simulation runs and optimizes the fault dictionary table.

Algorithm 1:
Step 1: First the circuit is analyzed for nominal values i.e. the circuit is simulated for nominal values.
Step 2: Each component values are varied by a certain percent (5% and 10%) at a time and the output value is found out.
Step 3: The variation in the output value is compared with the nominal values.
Step 4: The sensitivity of each component with respect to the output is calculated.
Step 5: The different values are then analyzed to find the component which has the maximum effect on the output.
Step 6: The component(s) which has the maximum sensitivity is called the Critical Component (‘s).
Step 7: The value of the critical component (‘s) is now re simulated for a variation in value which is less than the value taken earlier. This is done to recheck the critical components identified earlier.
The method proposed in this paper identifies critical components in the Circuit Under Test (CUT). This helps the manufacturer to take more precautions during manufacturing so that the tolerance is reduced and they are made more precise.

IV. CIRCUIT UNDER TEST (CUT)

The circuit used is a 2nd order Butterworth Filter and the multi frequency method is used as proposed by S.P. Venu, Sarat and Lal Kishore in [16]. As per this the frequency set chosen are those frequencies above and below the cut off frequency of the CUT chosen. The test frequency $\mathbf{f_T}$ set chosen is:

$\mathbf{f_T}$ = [500, 800, 1000, 1200, 1500].

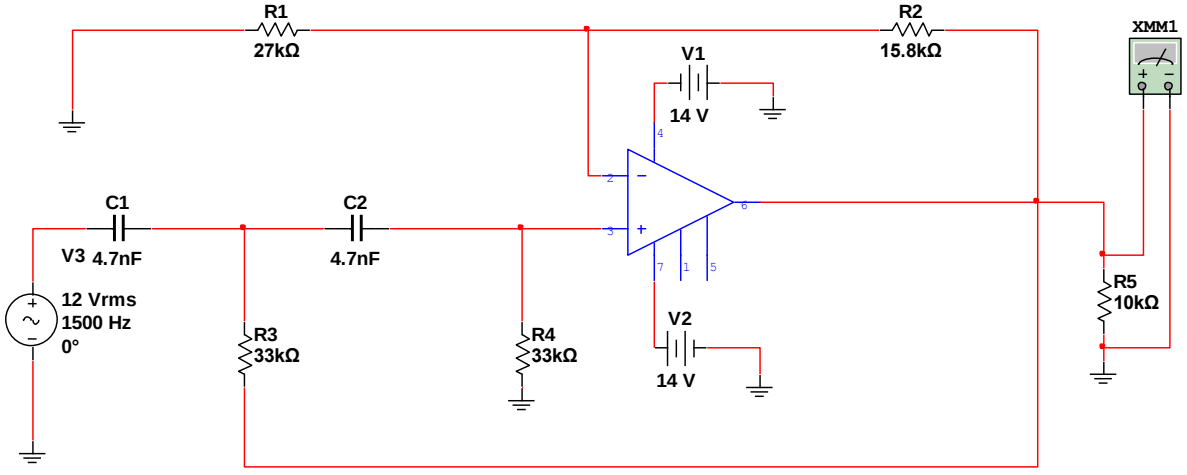

Figure: 2nd Order Butterworth Filter

The number of components in the given circuit is R_1, R_2, R_3, R_4, R_5, C_1 and C_2 (seven components). The circuit is simulated for both the nominal values and for a change in value (increase or decrease) by 10 % and 5% from the normal component values.

The types of faults associated with the corresponding names are given in Table 1.

Table 1: Fault Types

S. No	Fault Type	Name
1	Nominal	F_0
2	R_1 up 10%	F_1
3	R_2 up 10%	F_2
4	R_3 up 10%	F_3
5	R_4 up 10%	F_4
6	R_5 up 10%	F_5
7	C_1 up 10%	F_6
8	C_2 up 10%	F_7
9	R_1 down 5%	F_8
10	R_2 down 5%	F_9
11	R_3 down 5%	F_{10}
12	R_4 down 5%	F_{11}
13	R_5 down 5%	F_{12}
14	C_1 down 5%	F_{13}
15	C_2 down 5%	F_{14}

The CUT is simulated for both nominal condition and faulty conditions. The circuit values are changed to simulate the error in all the cases shown in table1. The reading of the circuit are tabulated in Table 2 and Table 3.

The actual readings of the filter are shown in Table 2 for a component variation increase of 10%.

Table 2.

Frequency	FAULTS							
	F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7
500	4.396	4.177	4.644	4.605	5.015	4.396	4.759	4.852
800	9.204	8.941	9.443	9.164	9.629	9.204	9.361	9.462
1000	9.89	9.75	10.024	9.83	10.097	9.89	9.943	9.995
1200	10.148	10.045	10.25	10.097	10.287	10.149	10.18	10.211
1500	10.339	10.258	10.42	10.304	10.432	10.34	10.361	10.377

The actual readings of the filter are shown in Table 2 for a component variation decrease of 10%

Table 3.

Frequency	FAULTS							
	F_0	F_8	F_9	F_{10}	F_{11}	F_{12}	F_{13}	F_{14}
500	4.396	4.672	4.155	4.132	3.819	4.396	4.01	3.939
800	9.204	9.467	8.912	9.222	8.432	9.204	8.968	8.8
1000	9.89	10.038	9.735	9.951	9.583	9.89	9.816	9.74
1200	10.148	10.26	10.034	10.205	9.953	10.148	10.107	10.06
1500	10.339	10.427	10.249	10.382	10.211	10.339	10.312	10.288

V. RESULTS

Sensitivity analysis has been carried out and the sensitivity of each and every component has been calculated. The sensitivity analysis results are shown in Table 4 for a component variation of increase in 10% and Table 5 for a component variation of 10% decrease.

Table 4: Sensitivity analysis for 10% increased variation in the component values.

Frequency	Sensitivity						
	S_1	S_2	S_3	S_4	S_5	S_6	S_7
500	**8.11**	**15.7**	**6.33**	**18.76**	**0**	**77.23**	**97.02**
800	**9.74**	**15.13**	**-1.21**	**12.88**	**0**	**33.4**	**54.89**
1000	**5.19**	**8.481**	**-1.82**	**6.273**	**0**	**11.28**	**22.34**
1200	**3.81**	**6.456**	**-1.55**	**4.212**	**0.1**	**6.809**	**13.4**
1500	**3.00**	**5.127**	**-1.06**	**2.818**	**0.1**	**4.681**	**8.085**

Table 5: Sensitivity analysis for 10% increased variation in the component values

Frequency	Sensitivity						
	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}
500	**10.2**	**15.25**	**8**	**17.48**	**0**	**82.13**	**97.23**
800	**9.74**	**18.48**	**-0.55**	**23.39**	**0**	**50.21**	**85.96**
1000	**5.48**	**9.81**	**-1.85**	**9.303**	**0**	**15.74**	**31.91**
1200	**4.15**	**7.215**	**-1.73**	**5.909**	**0**	**8.723**	**18.72**
1500	**3.26**	**5.696**	**-1.3**	**3.879**	**0**	**5.745**	**10.85**

Table 6: Average sensitivity of the Components

Sensitivity						
S_1	S_2	S_3	S_4	S_5	S_6	S_7
-6.270	**10.734**	**0.327**	**10.491**	**0.020**	**29.596**	**44.043**

As seen from these results it has been found that the most critical component is C_2. The other critical components in the descending order of criticality are C_1, R_4 and R_2. As such components are to be chosen precisely to prevent faults in the circuit. In this paper an algorithm has been proposed which identifies the most critical component of the circuit.

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