International Journal of
Emerging Research in Management &Technology
ISSN: 2278-9359 (Volume-5, Issue-8)

Research Article | **August 2016**

Effect of High-k Gate Dielectric Materials on Electrical Characteristics of GaAs Channel Material Based Double Gate n-FinFET

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Abstract:

This paper investigates the electrical characteristics of n-channel DG-FinFET structure and their sensitivity to gate dielectric materials with GaAs as channel material. The exercise of new channel material can improve the speed and performance of DG-FinFET because their higher electron mobility and device on-currents at low supply voltage. The influence and performance prospective of various high-k dielectrics such as SiO_2, SiON, HfO_2 and La_2O_3 as the gate oxide for a 12 nm GaAs based DG-FinFET has been explored and their impact on the electrical characteristics such as transconductance (g_m), threshold voltage (V_{th}), subthreshold swing(SS) and drain induced barrier lowering(DIBL) has been investigated. The results shows that high-k dielectric La_2O_3 exhibits the best material and can reinstate SiO_2, SiON, and HfO2 as it provides high transconductance, reduced sub-threshold swing , increased threshold voltage and reduced DIBL. The tool used to carry out simulation is PADRE simulator from MuGFET, which is based on the drift-diffusion theory and provides self consistent solution to the Poisson and drift-diffusion equations.

Keywords: FinFETs; Short channel effects (SCEs); Gallium Arsenide (GaAs); Lanthanum oxide (La_2O_3); Drain induced barrier lowering (DIBL); Subthreshold swing (SS).

I. INTRODUCTION

With the advancement in the microelectronic the new technology oriented towards the miniaturization of electronic components and transistors in integrated circuits. The goal is to integrate more components per unit area and thus improve circuit performance while lowering their manufacturing cost. Gordon Moore in 1965 predicted that the no. of transistors in a chip doubles every two years [1]. So, in order to keep pace with his statement the transistors size decreases from micrometer to sub-micrometer regime. The scaling of transistors can be reduced to below 20 nm to meet the predictions and goals set by the international technology roadmap for semiconductors (ITRS) [2]. As the device dimensions are scaled beyond the 16 nanometer regime, conventional single gate MOSFETs experience various short channel effects (SCE's) that deteriorate the drive current and lead to off-state leakages. So, an alternative device is needed that can overcome such effects without deteriorating the device performance.

The multi-gate transistors like FinFETs (Fin-Shaped Field Effect Transistors) are considered to be the best candidates to extend the use of CMOS technology beyond the barrier of 14 nm. Double-gate FinFET is considered one of the most promising device structures for future CMOS technology, which provides a better electrical control over the channel and thus allows increasing the device performances [3-5].

FinFET is basically a fin type FET structure and very frequently named as a double-gate transistor. It consists of a thin body of silicon wrapped by gate electrodes or poly silicon layer and the current flows in the channel from source to drain. FinFET has many advantages such as good scalability and excellent electrostatic control with promising performance for the present day nanoscale technology [6,7].

With scaling limits and the associated SCE's of FinFETs, it seems that additional scaling down of FinFET device structure will be much more complicated because of various practical limitations, such as gate leakage through hot carrier tunnelling, DIBL, SS, and threshold voltage roll-off, which can put a limit on scaling of the FinFET structures. As anticipated, while reducing the device dimensions in order to comply with the Moore's law and the ITRS roadmap further improvement in FinFET speed and performance at low power supply will be possible by using new channel material other than Si [8-10].

This paper presents the simulation study work of nanoscale double gate n-channel FinFET with channel made of GaAs. This study has been carried out for various gate dielectrics which are SiO_2, SiON, HfO_2 and La_2O_3. The impact of these gate dielectric materials on transconductance (g_m), threshold voltage (V_{th}), sub-threshold swing (SS) and drain induced barrier lowering (DIBL) has been investigated. After investigation it is observed that La_2O_3 gives best results among others gate dielectrics by suppressing short channel effects (SCEs) and also has an outstanding capability of enhancing the device performance.

II. DEVICE STRUCTURE AND SIMULATION TECHNIQUE

A 2-D view of device structure of FinFET used in the present simulation work is as shown in Fig.1, specifying various devices parameters undertaken for simulation study.

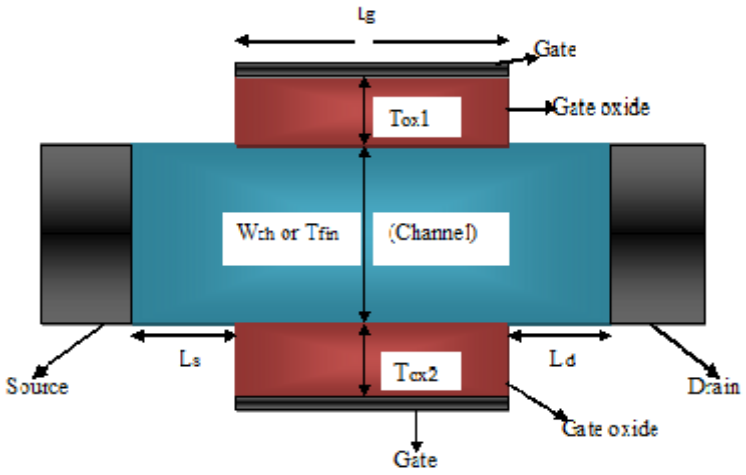

Fig.1. Two dimensional double-gate n-FinFET structure.

The various parameters of the above structure of FinFET can be defined as:

i) L_g: the gate or channel length between source and drain electrodes.ii) W_{ch} or T_{fin}: denotes the channel width which is separation between the either sides of fin. iii) L_s and L_d: extension length to source and drain. It determines the capacitance and significant source/drain resistance of the device. iv) T_{ox1} and T_{ox2}: thickness of the gate oxide material placed on the either side of the channel through which gate contact is made.

Further the channel is Gallium Arsenide material with N-type doping concentration of 1e+16 /cm^3, whereas doping concentration of drain/source is 1e+16/cm^3 and oxide thickness (t_{ox}) is 2 nm. The value of the gate contact work function is 4.6 eV and the band gap of GaAs is 1.424 eV at 300 K. In this present work, the device simulation has been carried out using PADRE simulator from MuGFET, which is based on the drift-diffusion theory and provides self consistent solution to the Poisson and drift-diffusion equations. The drift diffusion is being utilized for the device simulation, because of the fact that subthreshold characteristics of device are still diffusion dominated and reflect device characteristics in the subthreshold region and other results are reasonably well in consonance with the experimental results [11]. Infact, drift and diffusion simulations are significantly faster than quantum ballistic simulations and also fairly well fitted to experimental results. Moreover, it includes hot-carrier transport by solving energy balance equation and the velocity of carriers in the channel region is fitted to the Monte Carlo simulation results [12].

The associated high-k values for various gate dielectrics are shown in Table 1 and the parameters used for the present simulation work are shown in Table 2.

Table 1: Dielectric Constant Values for Various Dielectric Materials

Dielectric Materials	**Dielectric Constant (K)**
SiO_2	3.9
SiON	7.9
HfO_2	25
La_2O_3	30

As shown in table.1 the different dielectric materials with their associated dielectric constant (k), SiO2 is known as low-k dielectric material and responsible for high leakage current in FET devices. So, an alternative is needed which can give better outcome and overcome such drawback. However, analysis of different material has been done and Lanthanum oxide (La_2O_3) reveals that it can be better option as oxide material when compared to other.

Table 2: Parameters Used In Simulation

Device parameters	**Values**
Length of the gate (L_g)	12 nm
Equivalent oxide thickness (EOT) T_{OX1},T_{OX2}	2 nm
Fin width (W_{ch})	10 nm
Extension length to source/drain (L_s & L_d)	20 nm
Channel doping	1e+16/cm^3
Drain/source Doping	1e+19/cm^3
Channel doping type	N

The different parameters of the designed structure are shown in table.2, since different high-k dielectric materials are being considered to meet the improved result of various electrical characteristics of double gate n- FinFET, the choice of the material to be used as gate oxide in such devices will be depend on that which of the material provides improvement in the electrical characteristics of such device as according to device structure parameter variations. Also, basic channel material Si has been replaced by new channel material GaAs, in order to analyze and improve the transistor speed and performance at low power supply which is an important consideration.

III. RESULT AND DISCUSSION

In this section, various results pertaining to gate dielectric material such as SiO_2, SiON, HfO_2 and La_2O_3 for GaAs channel based DG-FinFET has been presented. The most important characteristics are threshold voltage (V_{th}), subthreshold swing (SS), drain induced barrier lowering (DIBL) and transconductance (g_m) have been investigated as these becomes prominent when the device dimensions shrinks.

A. Threshold Voltage (V_{th})

The main cause for threshold voltage roll off is charge sharing. When the device dimensions shrink the threshold voltage began to decrease as the charge in the depletion region is supported by drain and the source also. In this case the gate needs to support less charge in this region and as a result, V_{th} falls down, thereby degrading device performance. So, maintaining higher threshold voltage is the key requirement for low standby power [13]. Fig.2 shows the threshold voltage (V_{th}) variations for various high-k gate dielectrics. The threshold voltage values for SiO_2, SiON, HfO_2 and La_2O_3 are 0.18 V, 0.31 V, 0.41 V, and 0.42.5 V can be seen from graph. Among these materials the higher value of V_{th} is obtained for La_2O_3 resulting in improved V_{th}. The threshold voltage expression in case of a multigate FET device structure can be expressed as [13].

$$V_{th} = \Phi_{ms} + 2\Phi_f + \frac{Q_D}{C_{ox}} + \frac{Q_{ss}}{C_{ox}} + V_{in} \quad \textbf{(1)}$$

Where Φ_{ms} represents metal-semiconductor work function difference between the gate electrode and the semiconductor, Φ_f is the Fermi potential, Q_D is the depletion charge in the channel, C_{ox} is the gate capacitance and Q_{ss} represents charge in the gate dielectric.

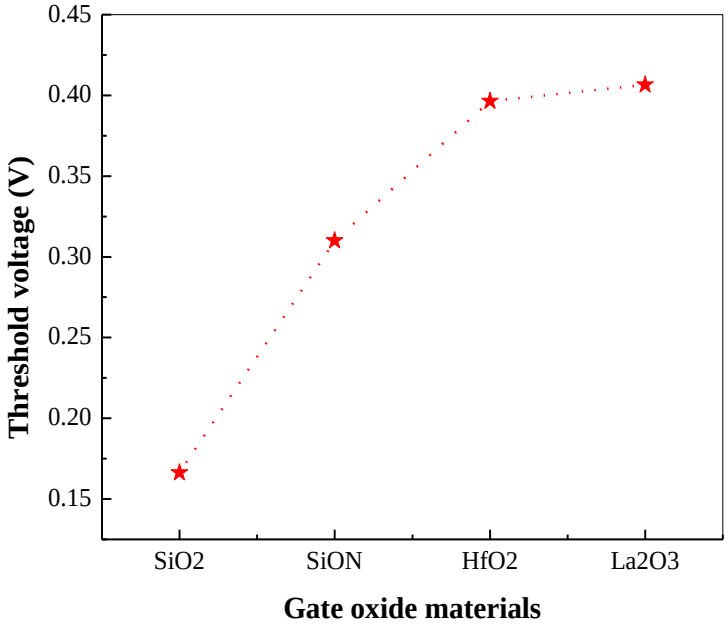

Fig. 2. Threshold voltage variation for different gate dielectric materials at V_D = 1 V

B. Subthreshold Swing (SS)

The subthreshold voltage is the major parameter for calculating the leakage current and it determine the holding time in dynamic circuits and static power dissipation in static CMOS circuits. For a MuGFET, the typical value for SS parameter is 60 mV/decade. The SS can be expressed by following equation [13]:

$$SS\ (mV/dec) = \frac{d\,V_{GS}}{d(\log_{10} I_{DS})} \quad \textbf{(2)}$$

Fig. 3 shows the subthreshold swing variation for different high-k dielectric materials at V_D = 1 V. The SS values for SiO_2, SiON, HfO_2 and La_2O_3 are found to be 118 mV/dec, 98 mV/dec, 90 mV/dec, 76 mV/dec, respectively. From graph it can be clearly seen that the subthreshold swing for La_2O_3 shows lowest values as a dielectric material with 76 mV/ dec, for GaAs based double-gate FinFET having gate length of 12 nm. The reason behind the reduced SS for La_2O_3 is its higher dielectric constant (~ 30) and reduced leakage current. Additionally, high-k value leads to increase in the capacitance between the channel and the gate, which results in less leakage current between drain and gate and further improves the subthreshold swing.

When a dielectric material is inserted between the metal gate and semiconductor material, the capacitance increases by the relative dielectric constant κ. In this case, the capacitance is described by [14]:

$$Cox = A\frac{k\varepsilon_o}{t_{ox}} \quad \textbf{(3)}$$

Where κ is the dielectric constant of the material (κ= ε/ε$_0$), ε$_0$ is the permittivity of free space, t_{ox} is the thickness of dielectric layer.

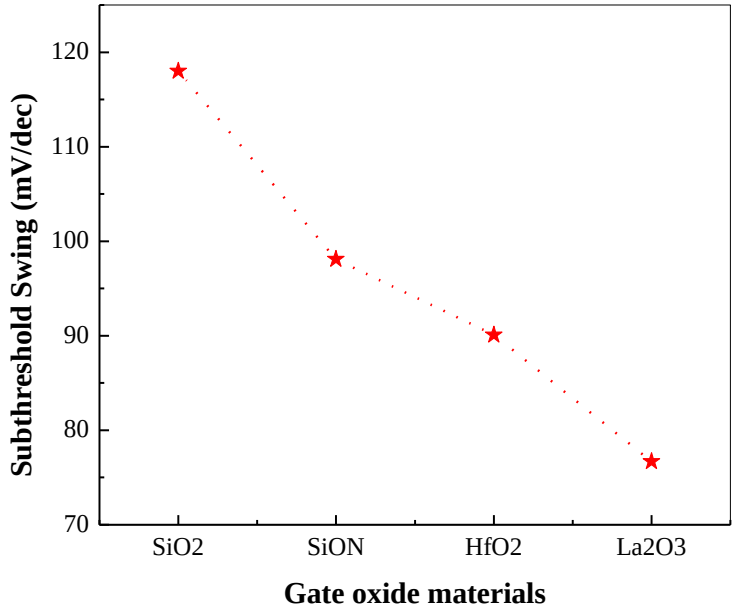

Fig. 3. Subthreshold slope variation for different gate dielectric materials at V_D = 1 V

C. Drain Induced Barrier Lowering (DIBL)

DIBL is one of the short channel effects and it is defined as the reduction in the potential barrier when the drain voltage is increased. For MuGFET devices it can be calculated as [14]:

$$\text{DIBL (mV/V)} = \frac{\Delta V_{TH}}{\Delta V_{DS}} \quad \textbf{(4)}$$

With the reduction in source junction barrier, electrons are easily injected into the channel and the gate voltage has no longer control over the drain current.

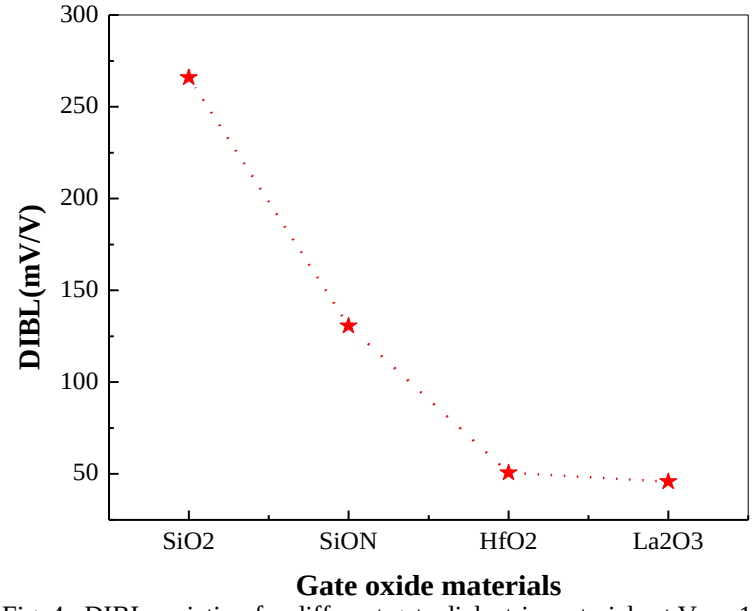

Fig. 4. DIBL variation for different gate dielectric materials at V_D = 1 V

Fig. 4 shows the DIBL variation for different high-k dielectric materials at V_D = 1 V. The DIBL values for SiO_2, SiON, HfO_2 and La_2O_3 are found to 267 mV/V, 131 mV/V, 51 mV/V and 47 mV/V respectively. La_2O_3 has shown minimum value among others. Higher value means less gate control so this value has to be reduced, as shown in graph with increased value of *k* the DIBL reduces. So, an alternate of SiO2 is needed and according to graph result La2O3 is best alternative as it has high value of *k*. That's why oxide materials having high dielectric constant values are preferred for nanoscale devices.

D. Transconductance (g_m)

In MOS devices transconductance relates the drain current to the gate voltage which is basically an analog circuit design parameter and can be calculated as [14]:

$$g_m = \frac{d\, I_D}{d\, V_{GS}} \quad \textbf{(5)}$$

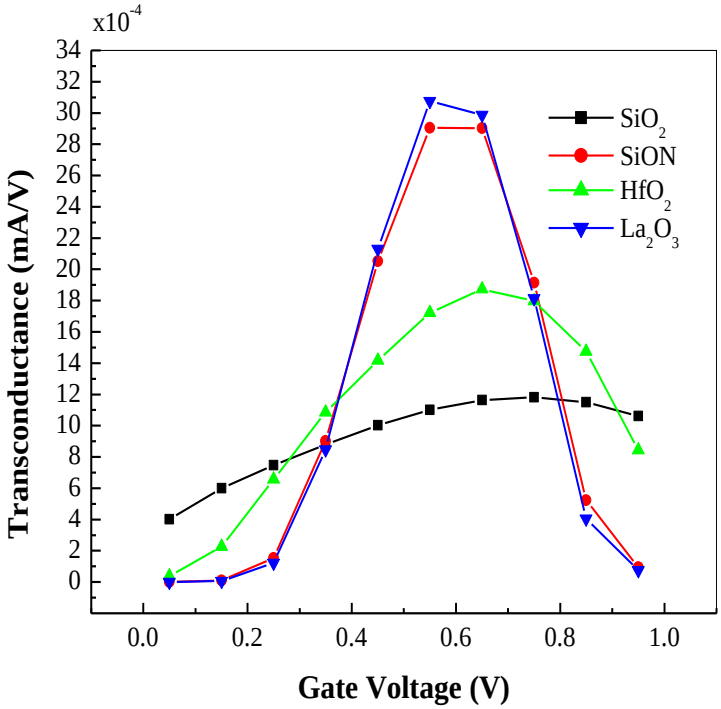

Fig. 5. Transconductance variation for different gate dielectric materials at V_D = 1 V.

Fig. 5 shows the transconductance variation with respect to gate source voltage for various high-k dielectric materials at V_D = 1 V. It can be seen that transconductance increase with the increase of dielectric constant. From the graph, it is clear that the values of transconductance for SiO_2, SiON HfO_2 and La_2O_3 are found to 11×10^{-4} S/µm, 19×10^{-4} S/µm, 31×10^{-4} S/µm and 32×10^{-4} S/µm respectively. It can be concluded that La_2O_3 shows increase for transconductance in comparison to other and has the potential of keeping drain current under control with respect to gate bias and further enables more rapidly carrier transport with 12 nm gate length when GaAs is taken as channel material.

IV. CONCLUSION

In this work, the PADRE simulator from MuGFET has been used to design and simulate GaAs channel material based DG-FinFET with different gate dielectrics for 12 nm node technology. GaAs based FinFET with La_2O_3 as gate dielectric demonstrates high transconductance, improvement in threshold voltage, reduced SCEs such as DIBL and subthreshold swing. Moreover, the nanometer gate device with La_2O_3 as gate dielectric shows better gate control, reduction of the leakage current which ultimately led microelectronic to new improved IC technology.

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