International Journal of Emerging Research in Management &Technology
ISSN: 2278-9359 (Volume-5, Issue-5)

Research Article | **May 2016**

Design and Implementation of High Speed 64 bit VEDIC Multiplier

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Abstract—

The need of high speed processing is increasing day by day on account of recent computer applications. As the multiplication takes considerably more amount of time for its calculation, the computation time must be reduced to get speedy results. To obtain the speedy results, either computation time must be reduced or the pace of the coprocessor must be improved. In this paper we proposed an efficient 64 bit multiplication making use of VEDIC multiplier to expand the pace of operation as when compared with the existing algorithms. Architecture of Vedic multiplier with less number of gates and high speed specification is designed here. Synthesis of the Implementation of this multiplier has been done on Xilinx XST.

Keywords— Computation time, gates, high speed, VEDIC multiplier, Xilinx.

I. INTRODUCTION

The pursuance of the processor is decided by its speed. For all the systems high speed processing is a necessitous requirement. Multiplication is a significant operation in Digital signal processors and ALU, and hence the demand for prime speed multiplication is continuously increasing in state-of-the-art VLSI design.

With the contemporary development of VLSI technology the demand for portable and embedded Digital signal Processing (DSP) methods has extended effectively. It is additionally the fastest developing science in this century and, as a consequence, as it creates vital challenges.

Faster multiplications and additions are very much significant in Signal processing, digital filters, discrete Fourier develops into and so on. Vedic arithmetic is the identity given to the historical method of arithmetic. We talk about feasible multiplier structure of Vedic arithmetic to be implemented on digital signal processing functions.

AlJuffri et.al [01] proposed a robust method for improving the performance of FIR filter by designing the efficient multiplier. This paper made use of Vedic multiplier and Wallace tree for the implementation of parallel and sequential micro programmed FIR filter architecture. Wen Naaz et.al [04] presented a design for Vedic multiplier using carry select adder. The design was proposed on the aim to reduce the propogation delay in the system. The design was then used in the FIR filters, which later proved to reduce the delay. Akanksha Pawar et.al [05] aimed at designing and implementing a fast multiplier using vedic mathematics which can be implemented in any processor application. Study on different bit multiplier is done here with less number of gates and with high specifications. The designing tool chosen here is Xilinx XST and Modelsim for simulation.

Dilip J Udhani et.al [06] proposed an approach for designing a high speed multiplier. The multiplication is based on vedic mathematics. This approach is more efficient while multiplying large numbers. 4x4 bit and 8x8 bit multiplier are considered in this flow. Neeraj Kumar Mishra et.al [07] developed a multiplier architecture based on crosswise and vertical structure of ancient Indian Vedic structure. The proposed work divides a 32 bit multiplicand and multiplier into MSB and LSB bits each of length 16 bit and this decomposition is given to a 16X16 multiplication. The synthesis is done using Xilinx Synthesis 16.1. Researchers in [08], [09] and [10] also proposed efficient methods using Vedic Multipliers. The proposed method made use of Vedic multiplication for designing 64 bit multiplier and the implementation is done in Xilinx.

II. METHODOLOGY

There are different sutras of multiplication followed in vedic arithmetic [02]. The proposed work made use of Urdhva-Tiryaghbhyam sutra. This is the multiplication formula applied to all the types of multiplication. The special property of this sutra is that it partially generates product and also performs addition simultaneously at the same time. This approach is more efficient in binary multiplication.

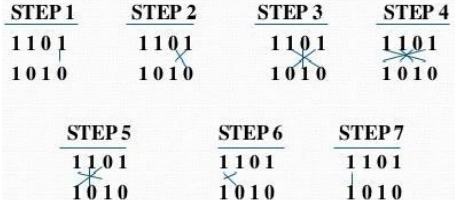

Figure 1: A Example for Urdhva-Tiryaghbhyam sutra using binary multiplication

In this multiplication approach, the inputs are divides into LSBs and MSBs, these two forms a combination of four and these four combinations are multiplied and added. As shown in the design, the carry generated from one adder is utilized in the other as per the flow. The carry out from the adders must not be neglected and must be added at a particular bit value. This leads to the generation of the bits of the carry and the result. The architecture of the proposed system is as shown in the Figure 2. The given architecture implements 64 bit Vedic multiplier using 32 bit multiplier using carry save adder [03]. Which use the structural programming style and implemented using Verilog HDL. The output of the 32 bit multiplier will go through 64 bit adder module to give the final product of 128 bits.

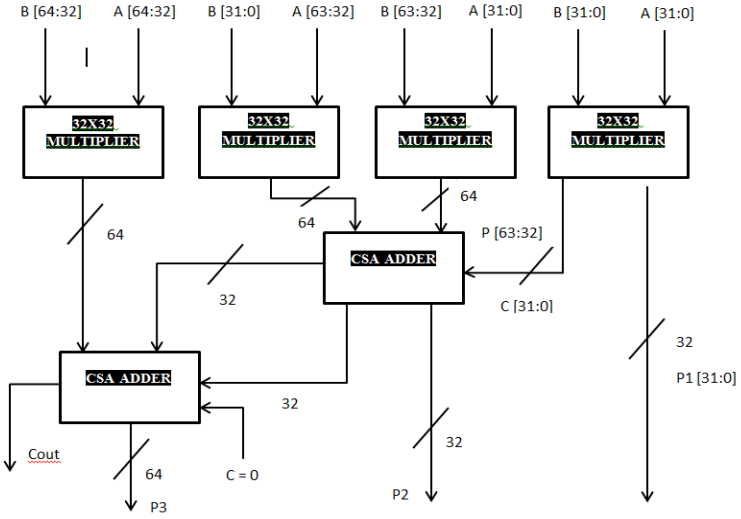

Figure 2: Block Diagram of the 64X64 bit Vedic Multiplication

III. EXPERIMENTAL RESULTS

The proposed 64 bit Vedic Multiplier is coded using Xilinx ISE Design Suite 13.2 and simulated using ISim (0.61xd) simulator. The simulated experimental result is shown in the figure below.

Case 1:-
Input A = 1234123412341234
Input B = 1234123412341234
Output S = 014B5D26B90214DD6E221246B66B5A90

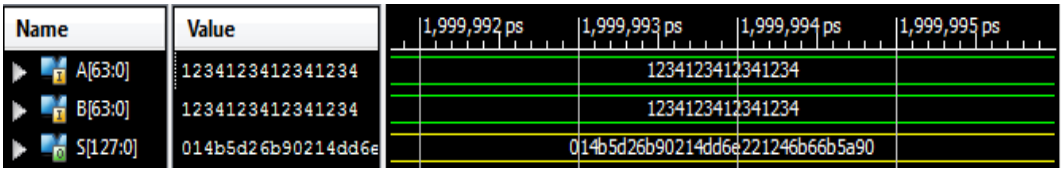

Figure 3: Simulation Result-1

Case 2:-
Input A = 1355732153214984
Input B = 6574516874352146
Output S = 07A97F4A3DD0D94CEE5EB3A80DE81E18

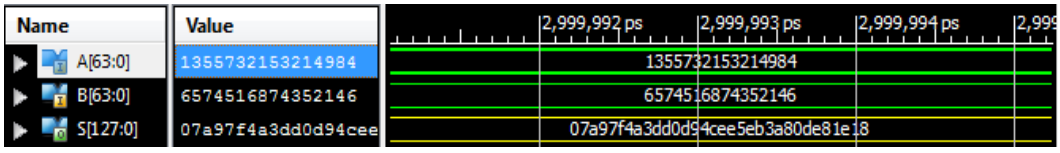

Figure 4: Simulation Result-2

Case 3:-
Input A = FFFFFFFFFFFFFFFF
Input B = FFFFFFFFFFFFFFFF
Output S = FFFFFFFFFFFFFFFE0000000000000001
Carry out = 1

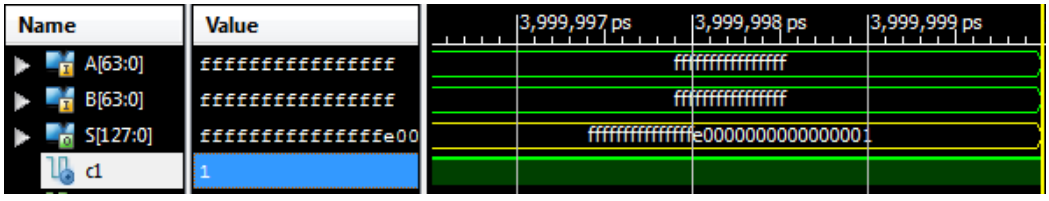

Figure 5: Simulation Result-3

IV. CONCLUSION

This paper presents a novel way of realizing high speed multiplier using Urdhva-Tiryagbhyam sutra and carry save addition technique. A 32 bit modified multiplier is designed. The 64 bit multiplier is realized using four 32 bit Vedic multipliers and two modified carry save adder. Vedic arithmetic deals with themes of arithmetic reminiscent of normal mathematics. The proposed architecture proves to be incredibly fast and accurate.

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