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High Speed Area Efficient 2×2 Fast Parallel FIR Filter using Common Boolean Logic

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Abstract:

In the advanced digital technology the need is of high speed in real time system along with the improvement in implementation issue. Vedic Multipliers has been used to solve the typical and tedious engineering calculation by simple Vedic methods. Here in this paper we have proposed the Vedic multiplier with Common Boolean Logic adder to improve the propagation delay time and area on silicon chip. With this slight improve in the multiplier, great results have been achieved in signal processing tasks. The VM has been designed for the target device XC3S400 -5 PQ208.

Keywords: Common Boolean Logic (CBL), Finite Impulse Response (FIR), Vedic Multiplier (VM)

I. INTRODUCTION

Due to the explosive growth of multimedia application, the demand for high-performance and low-power digital signal processing (DSP) is getting higher and higher. Finite-impulse response (FIR) digital filters are one of the most widely used fundamental devices performed in DSP systems, ranging from wireless communications to video and image processing. Some applications need the FIR filter to operate at high frequencies such as video processing, whereas some other applications request high throughput with a low-power circuit such as multiple-input multiple-output (MIMO) systems used in cellular wireless communication. Furthermore, when narrow transition-band characteristics are required, the much higher order in the FIR filter is unavoidable. For example, a 576-tap digital filter is used in a video ghost canceller for broadcast television, which reduces the effect of multipath signal echoes. On the other hand, parallel and pipelining processing are two techniques used in DSP applications, which can both be exploited to reduce the power consumption. Pipelining shortens the critical path by interleaving pipelining latches along the data path, at the price of increasing the number of latches and the system latency, whereas parallel processing increase the sampling rate by replicating hardware so that multiple inputs can be processed in parallel and multiple outputs are generated at the same time, at the expense of increased area. Both techniques can reduce the power consumption by lowering the supply voltage, where the sampling speed does not increase. In this paper, parallel processing in the digital FIR filter will be discussed.

The paper is organized as follows: Section II proposes the related work. Section III contains architecture of proposed Vedic multiplier using carry Boolean logic Section IV provides proposed methodology for Vedic multiplier. Section V contains results and discussion. Section VI conclusions followed by future work.

II. RELATED WORK

In general, two parallel FIR filter can be expressed as Traditional two parallel digital FIRS filter is shown in figure 1. For this two parallel FIR filter L=2. This will require three FIR sub-filter blocks of length N/2, one pre-processing adder and three post-processing adders. Total number of multiplier and adders required are 3N/2 and 3(N/2-1) + 4 respectively.

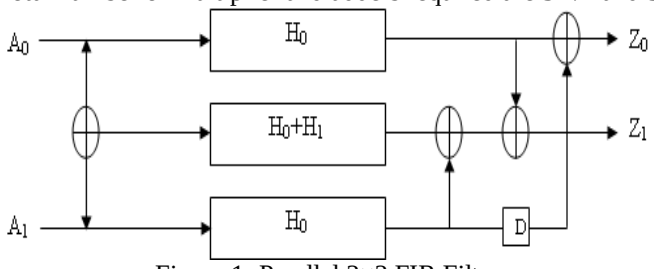


Figure 1: Parallel 2×2 FIR Filter

Following are the equations used to design the two parallel FIR filter with two inputs A0, A1 and two outputs Z0, Z1. For implementing this filter three FIR sub-filter blocks has been used as compare to traditional two FIRs sub-block filter, having length N/3. Two of three sub-filters H0+H1 and H0-H1 are having symmetric coefficient which reduces the number of multiplier and adders. Here two preprocessing and four post-processing adders have been used along with delay equipment. The symmetric sub-filter block has been implemented at the cost of two additional adders among those one is pre-processing and other one is post-processing for L=2.

Following are the equations used to design the filter:

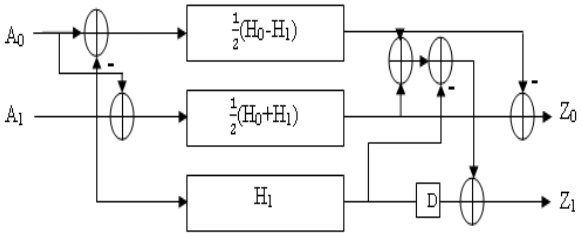


Figure 2: Proposed Parallel 2×2 FIR Filter

This same process is used for the n number of bits and thus we get the final sum and carry as output.
Example 1: Consider a 33-tap FIR filter with a set of symmetric coefficient as follows:
{h(0), h(1), h(2), h(3), h(4),…….....h(29), h(30), h(31)}
Where

h(0) = h(32),
h(1) = h(31),
h(2) = h(29),
h(3) = h(28)
……
h(12) = h(20)

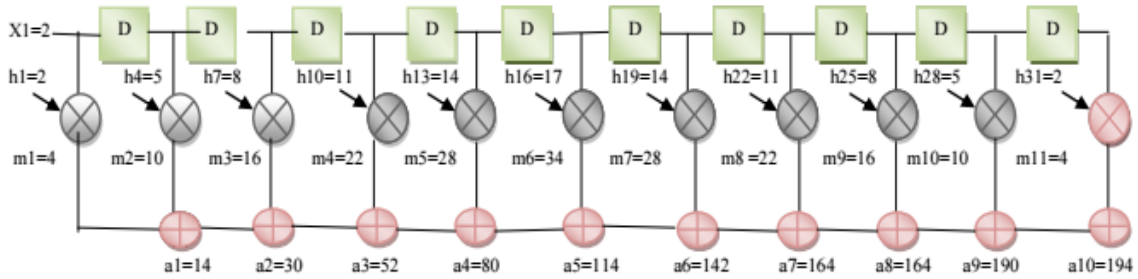


Figure 3: Internal Structure of H1

The symmetric parallel FIR filter is shown in Figure 2. The three parallel FIR filter consists of filter blocks. The input to the system is represented as A0, A1 and the response of the system as Z0 and Z1. Let X0=5, X1= 2, X2=3. The filter blocks H1 with its mod 3 coefficients are shown in Figure 3.
The proposed high speed Vedic multiplier is used in parallel FIR architecture. The proposed technique improves the speed of FIR filters and area utilization when compared to traditional Vedic multiplier.

III. PROPOSED ARCHITECTURE OF 16X16 BIT VEDIC MULTIPLIER

The multiplication of two numbers is done by using Urdhwa Triyakbhyam. Here first the least significant bits of the two digits are multiplied. Then the intermediate digits are cross multi-plied and added together. After this the most significant digits are multiplied.
For the 16X16 bit multiplication small block of 2X2 or 4X4 or 8X8 multiplier were used in parallel to make the process easy and efficient.

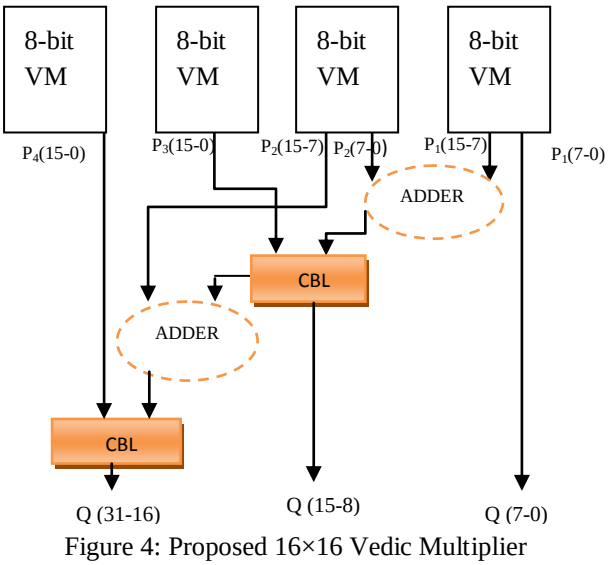


Figure 4: Proposed 16×16 Vedic Multiplier

In our proposed method the high speed carry select adder is replaced by the carry select adder along with Common Boolean logic which claims to provide a better speed and less propagation delay. Here we have used four multiplier of 8 bit to perform 16 bit multiplication. The method used is the addition of all partial product formed by the cross multiplication of one bit with another. The LSB bits of first multiplier P_1 (7-0) gives the LSB bits Q (7-0) of the final output. Another bits of first multiplier P_1 (15-8) are added in series with LSB 8 bits of second multiplier to form the 16 bits, which in turn get added with 16 bits of third multiplier by using CBL 1 Adder. The LSB bits of the output of CBL 1 adder forms the Q (15-8) bits of the final output. The remaining 8 bit P_2(15-8) is then added with the left 8 bits of CBL 1 output to from 16 bits, which is then added with 16 bits of the fourth multiplier by using CBL 2 adder. The output from CBL 2 adder forms the Q (31-16) bits. This is how the 32bit output is achieved in the less possible time.

IV. RESULTS AND DISCUSSION

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i updated version. Xilinx 9.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE™ (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 14.1i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution. ISE 14.1i Xilinx tools permits greater flexibility for designs which leverage embedded processors. The ISE 14.1i Design suite is accompanied by the release of chip scope Pro™ 14.1i debug and verification software. By the aid of that software we debug the program easily. Also included is the newest release of the chip scope Pro Serial IO Tool kit, providing simplified debugging of high-speed serial IO designs for Virtex-4 FX and Virtex-5 LXT and SXT FPGAs. With the help of this tool we can develop in the area of communication as well as in the area of signal processing and VLSI low power designing.

Table I: Comparison Results of Existing and Proposed Vedic Multiplier

XC3S400 -5 PQ208	Existing Vedic multiplier	Proposed Vedic multiplier
Delay	40.83ns	39.10ns
Number of Slices	445 out of 3584 (12%)	371 out of 3584 (10%)
Number of 4input LUTs	777 out of 7168(10%)	659 out of 7168 (9%)
Number of bonded IOBs	64 out of 141 (45%)	64 out of 141 (45%)

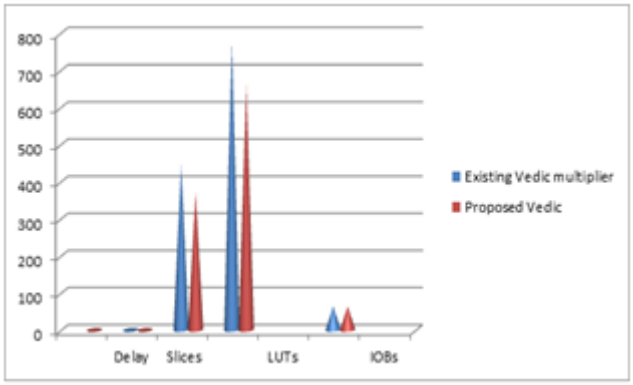
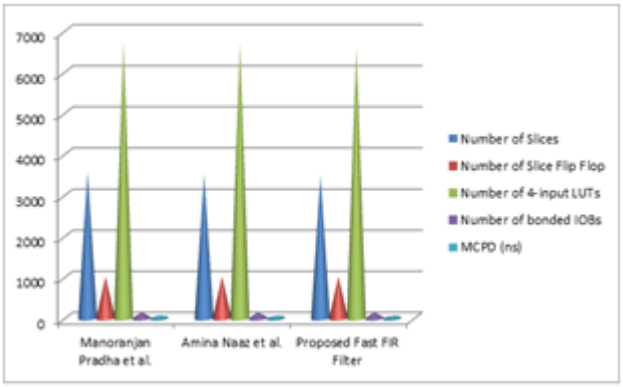


Table 2: Comparisons Result for different types of proposed design and different types of device family

Proposed Design	Number of Slices	LUTs	IOBs	MCPD (ns)
Manoranjan Pradha et al.	3582	6693	146	73.682
Amina Naaz et al.	3517	6682	146	58.924
Proposed Fast FIR Filter	3482	6586	146	52.682



V. CONCLUSION

The proposed 16x16 Vedic multiplier architecture has been designed and synthesized using on Spartan 3 XC3S400 board and is used in parallel FIR filter design. The proposed Vedic
Multiplier with carry select adder is compared with the existing Vedic multiplier using Carry select adder along with Common Boolean Logic and can be inferred that proposed architecture is faster compared to existing Vedic multiplier. In future the proposed multiplier performance parameters can be improved by high level pipelining operations and applied in signal processing applications like image processing and video processing.

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