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Research Article

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FPGA Realization of Multi-Port Memory Controller for Communication with DDR2 Memory

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Abstract —

In real time applications there is a need of memory for data storage. FPGA processor to the DDR2 memory communication can be carried out with the help of multi-port memory controller. The main features of FPGA processor are fast speed, flexible use and strong characteristics of reconfiguration. Multi-port memory controller supports DDR3/DDR2/DDR/SDRAM memories and it can be configured according to their requirements. It provides access to memory for one to eight ports where each port can be chosen with different interface modules. Multi-port memory controller provides direct memory access without interference of the processor. This communication is useful in real time applications for large data transfer requirement and high speed requirement.

Index Terms— MPMC, FPGA, DDR2, MicroBlaze real time

I. INTRODUCTION

Embedded systems with system on chip have an increasing demand for multiport memory controllers for higher system performance and energy efficiency. Traditional microprocessors have memory controllers on their motherboards but modern microprocessors have an integrated memory controller to reduce memory latency. These integrated memory controllers have potential to increase system performance. Embedded processors are available inside FPGA as hard IP or soft IP cores. It is possible to implement parallel logic for memory communication by using these processors and IP cores. FPGA processors can be used for programmable logic blocks and reconfigurable interconnects. These are useful in implementing complex digital logics. DDR2 memories provide double data rates by transferring data on both clock edges. These are high speed and low power memories. Multi port memories provide interface with such memories with multiple ports and various data bus sizes. Also they form FPGA FIFO interfaces for data read-write operations. On chip memories are not sufficient in size for real time applications so fast and flexible external large size memories are preferred which also provide flexible data rates.

II. MICROBLAZE PROCESSOR

MicroBlaze processor is a soft core processor which is part of a FPGA and can be introduced in the design by using Embedded Development Kit platform. MicroBlaze processor uses processor local bus for communication with other IPs. It works with big endian reversed bit format and 32-bit general purpose registers. A MicroBlaze system can range from processor core with a minimum of local memory to a large system with external memory controllers and different peripherals. Using the EDK platform a project can be created in Xilinx platform studio. The project includes instantiation of MicroBlaze processor, processor local bus and other peripherals. When hardware cores need high bandwidth and low latency transfers to off-chip memory, Xilinx provides a custom interface to their multi-ported memory controller (MPMC) known as then native port interface (NPI).This is different than a bus master, in that, it is a direct connect interface to the memory controller instead of a connection to a shared bus the memory controller so operating frequency, which can be higher than the bus operating frequency, providing a higher bandwidth.

III. FIFO (IP CORES)

A FIFO, or queue, is useful as buffer to capture data as it arrives from the producer and to allow the consumer to retrieve data, in order, at its convenience. Asynchronous FIFO uses control logic to perform read & write operation. Also it uses status flag, optional handshaking signal for interfacing with user logic. For the IP core FIFO two types of memories are available, Block RAM or shift register lookup RAM. With the help of block RAM better timing approach obtained so in most cases block RAM gives best results compared to shift register lookup RAM. When MPMC has large number of ports at that moment SRL RAM gives better results than block RAM. This FIFO's can support FULL, EMPTY, ALMOST_FULL & ALMOST_EMPTY flags. Invalid request cannot corrupt FIFO status. The CoreGen FIFO Generate or wizard presents a number of choices as to how a FIFO will be implemented in the FPGA fabric. The choices include Block RAM, distributed RAM, shift register(s),and built-in FIFO(s)if supported by the device.

IV. BLOCK DIAGRAM

4.1 Test Data Generation

This block contents logic to generate test data pattern, to assert write enable and read enable commands to FIFOs. Whole reset is also driven by that logic. This process also generates the next valid NPI address after a successful transaction has been made.

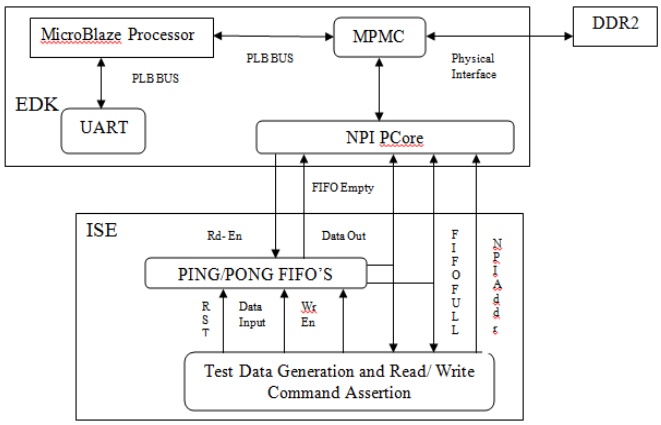

Fig.1. Block Diagram

4.2 FIFOs

First In First Out (FIFO) element is Xilinx-specific hardware component (dedicated IP core) by the Xilinx Core Generator used for clock domain synchronization between the incoming data clock (test data as of now) and the FPGA internal reference clock. Writing of data into FIFO is controlled by the Logic drive and reading of data is done by the specific process written in NPI Pcore logic. FIFO gives different flags i.e. full, empty to provide information of its status and accordingly read/write transactions takes place.

4.3 NPI PCore

Native Port Interface Personality index module (NPI PIM) is an interface to data access to memory which provides high speed transactions and low read/write latencies. NPI interface performs similar behaviour as a Direct Memory Access (DMA) device which writes the samples by means of NPI transactions without the need of the MicroBlaze Processor.

4.4 MPMC

The Multi Port Memory Controller (MPMC) provides access to the 1024 MB DDR2 memory, available on the board with 2 out of the 8 ports are configured to allow simultaneous access of NPI Pcore and Micro Blaze Processor. The NPI port provides the highest performance burst transaction of the port types supported by the MPMC .

4.5 Micro Blaze Processor

In this project a MicroBlaze soft core processor is used. It is a 32 bit RISC processor optimized by Xilinx FPGA. It is a reconfigurable soft core which has fixed as well as configurable features. It has 32 bit general purpose registers, 32 bit address bus and single issue pipeline.

4.6 UART

The UART core is a IP core used in EDK for the communication with Micro Blaze processor and PC. It communicates with Micro Blaze through processor local bus and transfers data read from memory to PC using hyper terminal.

4.7 DDR2

Here external DDR2 memory is used. This DDR2 memory can handle large amount of data With double data rate and low power efficiency. The DDR2 pins are interfaced with FPGA for communication.

V. IMPLEMENTATION AND RESULTS

The modules are implemented using Xilinx ISE and EDK platforms. The test data generation and FIFO modules are implemented in ISE and other modules in EDK environment. The generated data is written in FIFOs alternately and data is read from the FIFOs by using NPI. This read data is written into DDR2 with the help of multi-port memory controller. The written data into memory is again read back and then transferred the same to PC through UART module with the help of MicroBlaze processor. The write data and read data are compared and also speed of the communication is calculated based upon number of clock cycles, data width and burst size of data.

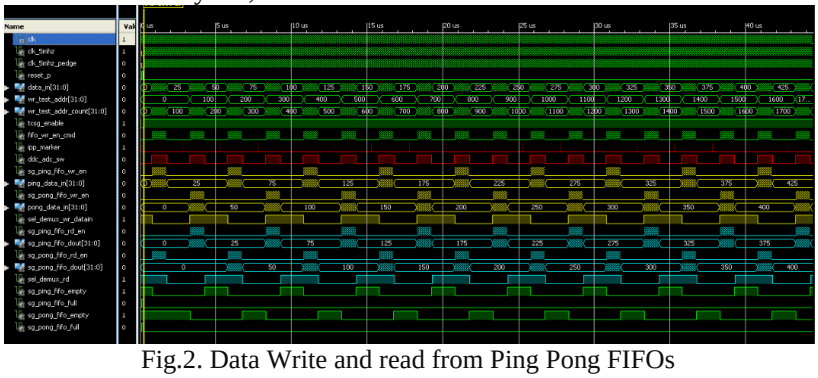

Fig.2. Data Write and read from Ping Pong FIFOs

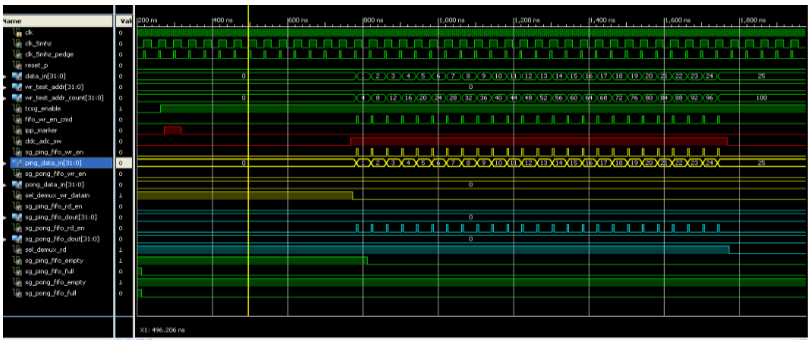

Fig.3. write en/read en and write /read data from FIFO

VI. CONCLUSION

The data write and read from the DDR2 is supported in the burst format with the use of multiple memory controller ports and different data sizes. Also Multi-port memory provides the flexible interface to the DDR2 memory with high speed using 100 MHz clock speed. The NPI port provides the highest performance burst transaction of the port types supported by the MPMC. The performance requirements for NPI port must be carefully considered. The interface will be useful for support in ever increasing demands on resolution, bandwidth, and buffer length for burst data capture.

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