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Research Article

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Design of Efficient and Fast Multiplier Using MB Recoding Techniques

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Abstract—

In Digital Signal processing applications, fast processing of a huge quantity of data in Digital form. Presently, multiplier plays a major role in Digital Signal Processors. Using three different schemes in Fused Add-Multiply (FAM) design for the reduction in terms of power and delay. Multiplier results of 7 bit and 11 bit (odd) for both signed and unsigned numbers to be produced using efficient modified booth recoding (EMBR) techniques in three different schemes of FAM design.

Keywords— EMBR, FAM, partial products, carry save adder, carry look ahead adder.

I. INTRODUCTION

In earlier days, the multiplication was executed via a sequence of addition and shift operations. These days, computer electronics make wide use of Digital Signal Processing, based on large number of arithmetic operations. Multiplication is one of them, can be reflected as successive additions. The number to be added is the multiplicand, the number of times added is the multiplier, and the result is the product. Multiplication includes two basic operations - generation of partial products plus their accumulation. Performance of system depends on multiplier. Final Carry Look Ahead (CLA) [6] adder and the Carry Save Adder (CSA) [6] tree used for quickness.

II. MOTIVATION

The carry propagation is overwhelming, and must be repeated for each partial product to be summed. Such a technique was first proposed by Booth [2]. The original Booth's algorithm crafts over contiguous strings of l's by using the property that: 2 +2(n-1) + 2(n-2) + . . . + 2hm) = 2(n + l) - 2(n-m). Although Booth's algorithm yields at most N/2 encoded partial products from an N bit operand, the number of partial products produced differs. Due to this, modified versions of Booth's algorithm are designed and simulated using Xilinx for low power applications.

III. MODIFIED BOOTH

Modified Booth (MB) is used in multiplication. Booth to Modify generates at most n/2+1 partial product. Advantage is that it reduces by half the number of partial products in multiplication relating to any other radix-2 representation.

Algorithm

1. Pad the LSB with one zero.
2. Pad the MSB with 2 zeros if n is even and 1 zero if n is odd. Divide the multiplier into overlapping groups of 3-bits.
3. Determine partial product scale factor from modified booth to encoding table.
4. Compute the Multiplicand Multiples.
5. Summing Partial Products.

TABLE I GROUPING TABLE

y_{2j+1}	y_{2j}	y_{2j-1}	y_j^{MB}	s_j	one_j	two_j	c_{inj}
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	2	0	0	1	0
1	0	0	-2	1	0	1	1
1	0	1	-1	1	1	0	1
1	1	0	-1	1	1	0	1
1	1	1	0	1	0	0	0

$one_j = y_{2j-1} \oplus y_{2j}$ $\quad two_j = (y_{2j+1} \oplus y_{2j}).\overline{one}_j$ $\quad s_j = y_{2j+1}$

Encoding can be done by looking at three bits at a time and must be able to add multiplicand times –2, -1, 0, 1 and 2. Since Booth recoding [4] got rid of 3's, generating partial products is not that hard. After the grouping of

partial products, they are added, weighted properly, through a Carry-Save Adder (CSA) [6] tree. Carry – Save. Followed by carry look ahead adder, Carry Look Ahead adder (CLA),a carry signal will be generated in two cases: (1) when both bits a and bare 1, or (2) when one of the two bits is 1 and the carry-in is 1. The Carry Look Ahead adder (CLA) [6] resolves the carry delay problem by computing the carry signals in advance, centred on the input signals. This addition reduces all partial-products down to a carry-save number by summing them up in an adder tree.

IV. SUM TO EFFICIENT MODIFIED BOOTH RECODING TECHNIQUE (S-MB)

A. Structured Signed Arithmetic

To reduce the number of partial products to be summed, both conventional and signed HAs and FAs are used [1] [2], each of the three schemes can be easily applied in either signed or un-signed numbers which consist of odd or even number of bits. In the following techniques, both inputs are in form for signed and unsigned consist of bits 2k in case of even or 2k+1 bits in case of odd bit-width considered. In S-MB recoding technique, recoding the sum of two consecutive bits of the input A (a2j, a2j+1) with two consecutive bits of the input B (b2j, b2j+1) into one MB digit Y_j^{MB}. Here, two types of signed HAs used which are referred as HA* and HA**. Truth tables and corresponding Boolean equations in [1].

$$Y = A + B = y_k . 2^{2k} + \sum_{j=0}^{k-1} y_j^{MB} . 2^{2j} \qquad (1)$$

Where $y_j^{MB} = -2\, s_{2j+1} + s_{2j} + c_{2j}$.

B. S-MB Recoding Techniques

1) Signed Input Numbers: If the input numbers A and B are signed, their MSB is negatively signed. Below represents are S-MB schemes for odd bit-width of A and B. The basic recoding block in all schemes remains unchanged.

a) SMB1 recoding scheme

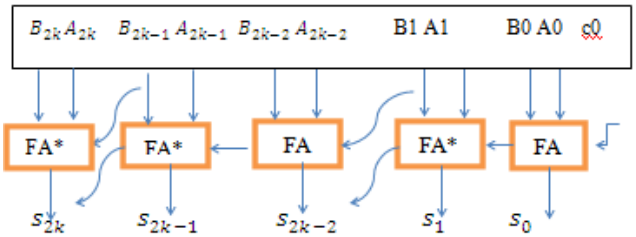

Fig. 1 Signed S-MB1 Odd number of bits.

b) SMB2 recoding scheme

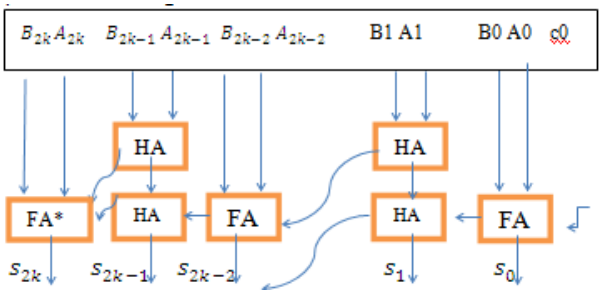

Fig. 2 Signed S-MB2 Odd number of bits.

c) SMB3 recoding scheme

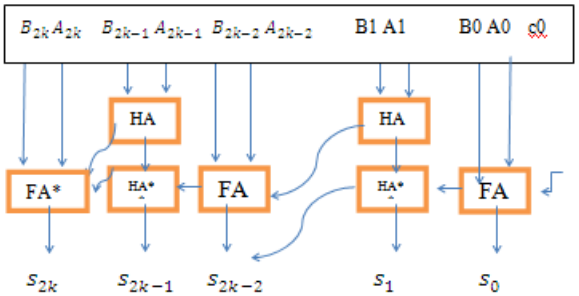

Fig. 3 Signed S-MB3 Odd number of bits.

2) Unsigned Input Numbers: If the input numbers A and B are unsigned, their most significant bits are positively signed. The basic recoding block in all schemes remains unchanged. Below represents are S-MB schemes for odd bit-width of A and B.

a) SMB1 recoding scheme

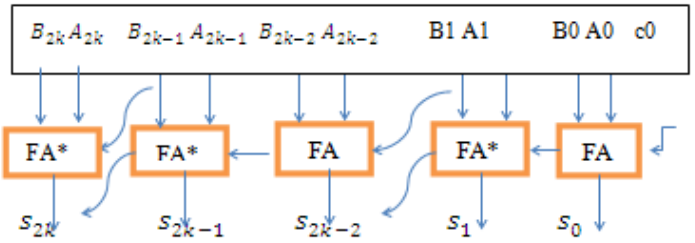

Fig. 4 Unsigned S-MB1 Odd number of bits.

b) SMB2 recoding scheme

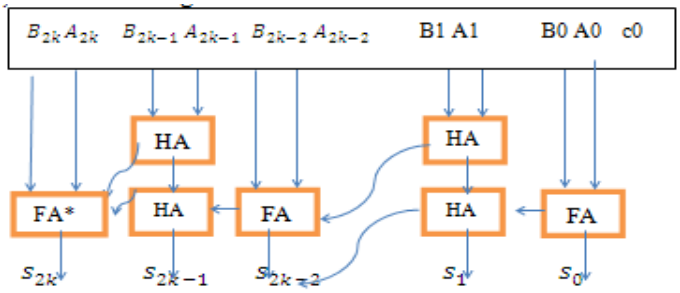

Fig. 5 Unsigned S-MB2 Odd number of bits.

c) SMB3 recoding scheme

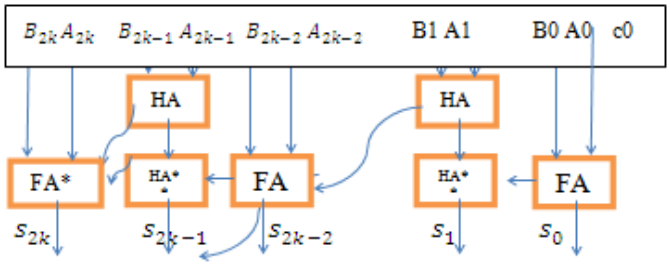

Fig. 6 Unsigned S-MB3 Odd number of bits.

V. FUSED ADD MULTIPLY IMPLEMENTATION

FAM design represented in Figure 7, the multiplier is a parallel one depends on the MB algorithm. Let us consider the product X. Y. The term Y = $(y_{n-1}y_{n-2}\cdots y_0)$ 2's is encoded based on the MB algorithm [1] [2] and multiplied with X = $(x_{n-1}x_{n-2}\cdots x_0)$ 2's. Both X and Y consist of n=2k bits and are in 2's complement type. Equation (2) describes the generation of k partial products:

$$PP_j = X \cdot y_j^{MB} = \bar{p}_{j,n}^{\,n}2 + \sum_{i=0}^{n-1} p_{j,i} \cdot 2^i \qquad (2)$$

The generation of the i- th bit $p_{j,i}$ of the partial product PP_j is given by next expression (3)

$$p_{j,i} = ((x_i \oplus s_i)one_j) + ((x_{i-1} \oplus s_j) + two_j) \qquad (3)$$

After generation of partial products, they are added, suitably weighted, through a Wallace Carry-Save Adder (CSA) tree along with the Correction Term (CT) which is specified by the following equation (4):

$$Z = X.\ Y = CT + \sum_{j=0}^{k-1} PP_j \cdot 2^{2j} \qquad (4)$$

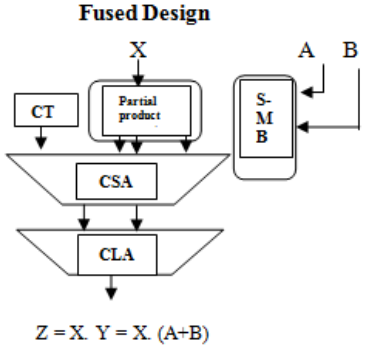

Fig. 7 Fused Design

VI. RESULT

The EMBR based multiplier in FAM is designed and simulated using Xilinx 14.2 simulator. The performance comparison of power and delay of all three recoding schemes for both signed, unsigned of 7, 11 (odd bit widths) bits multiplication results are tabulated.

Signed odd bit width

TABLE II. SIGNED MUL_SMB1

Mul_SMB1	7bit	11bit
Power(mw)	1.261	2.566
No of LUT's	145	295
Delay(ns)	19.469	23.285
Memory(kb)	256152	261088

TABLE III. SIGNED MUL_SMB2

Mul_SMB2	7bit	11bit
Power(mw)	1.209	2.479
No of LUT's	139	285
Delay(ns)	19.226	23.058
Memory(kb)	256472	261536

TABLE IV. SIGNED MUL_SMB3

Mul_SMB3	7bit	11bit
Power(mw)	1.269	2.609
No of LUT's	146	300
Delay(ns)	19.742	23.077
Memory(kb)	256664	261636

Unsigned odd bit width

TABLE V. UNSIGNED MUL_SMB1

Mul_SMB1	7bit	11bit
Power(mw)	1.209	2.174
No of LUT's	139	133
Delay(ns)	19.469	22.305
Memory(kb)	255776	259480

TABLE VI. UNSIGNED MUL_SMB2

Mul_SMB2	7bit	11bit
Power(mw)	0.765	0.991
No of LUT's	88	114
Delay(ns)	17.689	17.775
Memory(kb)	255456	255768

TABLE VII . UNSIGNED MUL_SMB3

Mul_SMB3	7bit	11bit
Power(mw)	0.782	1.644
No of LUT's	90	189
Delay(ns)	19.576	18.908
Memory(kb)	256008	255698

VII. CONCLUSION

In this paper, the efficient multiplier (Mul_SMB2) with EMBR Techniques using fused add-multiply is suggested. The design of 7 bit and 11 bit signed, unsigned multiplication displays significant improvement in the power consumption and delay. According to results, Mul_SMB2 is the effective one than other two schemes of both signed and unsigned in terms of power analysis and delay. Hence, due to better delay and power efficiency, this can be used in the Low Power applications. In future, it can be designed for more number of even and odd bit widths.

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