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An Adiabatic Approach to Design Low Power Energy Efficient CMOS Circuits

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Abstract-

Studies different sources of the power dissipation and evaluates a technique to reduce the power dissipation to much more extent. The need of devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies. Digital CMOS integrated circuits are important element of electronic system for achieving high performance. The demand for digital CMOS integrated circuits will continue to increase in the future, because of its important features such as low power, good reliability and other improvements in the processing technology. An ADIABATIC approach is perfect solution for the design of power and energy efficient designs.

Keywords— Digital CMOS circuit, EDA Tanner tool kit, T- SPACE tool,

I. INTRODUCTION

From the past few decades, VLSI technology has been growing to the large extent. All credit for this goes to the use of integrated circuits in embedded systems, mobile technology, computing system, etc. With ever increasing growth of technology, the demand for low-power consumption is also increasing. Due to high power consumption not only reliability of device is reduced but it also makes packing and cooling of device difficult. As a result cost of device increasing. Furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive.[3] Thus, power consumption becomes a major limitation for number of electronic systems

1.1 Principle Of Adiabatic Circuits

The term "adiabatic" refers to a thermodynamic process that exchanges no energy with the environment, and hence no energy or power dissipation occurs. Adiabatic technology is used to reduce the power or energy dissipation during the switching process and further reuse some of the energy by recycling it from the load capacitance [4][5].

- For reusing the energy, the adiabatic circuit uses the principle of Constant current source power supply
- For reducing power dissipation it uses the principle of Trapezoidal or sinusoidal power supply voltage.

II. PROPOSED WORK

The proposed modus-operand of this project is as follows:

The implementation of the Logical Circuits will be done in Tanner EDA Tool using CMOS and with the Adiabatic Logic. With the S-Edit tool of Tanner EDA the schematic of two-input NOT and NOR gate, 2*1 MUX and 1 bit Full Adder will be simulated by the T-SPICE tool.

- The Conventional CMOS NOT Gate with the constant V_{DD}
- The Adiabatic (PFAL) CMOS NOT Gate with the sinusoidal Power Pulse
- The Conventional CMOS NOR Gate with the constant V_{DD}
- The Adiabatic (PFAL) CMOS NOR Gate with the sinusoidal Power Pulse
- The Conventional CMOS 2*1 MUX with the constant V_{DD}
- The Adiabatic (PFAL) CMOS 2*1 MUX with the sinusoidal Power Pulse
- The Conventional CMOS Full Adder with the constant V_{DD}
- The Adiabatic (PFAL) CMOS Full Adder with the sinusoidal Power Pulse

Simulate the results using the both techniques and minimize the power dissipation: After designing and simulating the circuits, both designs are compared. And hence proved that power consumed by adiabatic CMOS circuits are very small as compared conventional CMOS circuits.

The comparison is discussed as

- In the Conventional CMOS of NOT gate, NOR gate, 2*1 MUX and Full Adder the V_{DD} is taken as a constant DC source, The value of the DC source is taken as 1.8V for NOT gate, NOR gate and Full adder while 2.5V for 2*1 multiplexer. The circuits are simulated in the T-SPICE of Tanner EDA.

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- In the Adiabatic circuits, the voltage source is taken is the Sinusoidal power clock. This power clock takes amplitude of 1.8V with 0V offset and 50MHZ of frequency. The circuits are designed using the Positive Feedback Adiabatic Logic; the reconstruction of the circuit is done from conventional circuit.

III. RESULTS AND DISCUSSION

All the design structures based on Conventional CMOS Logic and Adiabatic Switching Logic are designed and simulated using standard TSMC 90nm CMOS technology and at an operating frequency of 50MHz. Tanner EDA v13 schematic based tool known as S-EDIT have been used for designing the schematic of circuits. The analyses of the circuits are done in T-SPICE of Tanner EDA v13. The resultant waveform of the output is displayed in waveform editor of Tanner EDA known as W-EDIT. The basic circuits such as, NOT gate, Two-Input NOR Gate, Two-to-One Multiplexer, One-Bit Full Adder are designed and analyzed with appropriate sizing of the transistors.

Table 4.1: Comparison between Power Results Of NOT GATE Circuits

NOT GATE	**BASE PAPER RESULTS**	**PRESENT RESULTS**
SIMULATION CONDITIONS	1.8V :- voltage source 0.05pF :- capacitance 50MHz :- frequency	1.8V : - voltage source 0.05pF :- capacitance 50MHz :- frequency
TECHNOLOGY USED	180nm	90nm
POWER RESULTS (conventional)	7.9551340mw	4.223813mw
POWER RESULTS (PFAL)	4.6579418mw	1.318593mw

Table 4.2: Comparison between Power Results Of NOR GATE Circuits

NOR GATE	**BASE PAPER RESULTS**	**PRESENT RESULTS**
SIMULATION CONDITIONS	1.8V :- voltage source 0.05pF :- capacitance 50MHz :- frequency	1.8V : - voltage source 0.05pF :- capacitance 50MHz :- frequency
TECHNOLOGY USED	180nm	90nm
POWER RESULTS (conventional)	9.1454464mw	8.866097mw
POWER RESULTS (PFAL)	6.9542012mw	4.136027mw

Table 4.3: Comparison between Power Results of 2*1 MULTIPLEXER Circuits

MULTIPLXER	BASE PAPER RESULTS	PRESENT RESULTS
SIMULATION CONDITIONS	2.5V :- voltage source 0.02pF :- capacitance 50MHz :- frequency	2.5V : - voltage source 0.02pF :- capacitance 50MHz :- frequency
TECHNOLOGY USED	180nm	90nm
POWER RESULTS (conventional)	2.2e-7mw (0.0000022)	9.5e-8mw (0.00000095)
POWER RESULTS (PFAL)	2e-8mw (0.00000002)	7e-9mw (0.000000007)

Table 4.4: Comparison between Power Results of Full Adder Circuits

2*1 MULTIPLEXER	**BASE PAPER RESULTS**	**PRESENT RESULTS**
SIMULATION CONDITIONS	1.8V :- voltage source 0.05pF :- capacitance 50MHz :- frequency	1.8V : - voltage source 0.05pF :- capacitance 50MHz :- frequency
TECHNOLOGY USED	180nm	90nm
POWER RESULTS (conventional)	21.546534mw	19.87048mw
POWER RESULTS (PFAL- SUM)	13.64454mw	9.86526mw
POWER RESULTS (PFAL- CARRY)	7.654049mw	3.046574mw

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Table 4.5: Comparison between Power Results of Conventional and PFAL Circuits

CIRCUITS DESIGNED	CONVENTIONAL	PFAL
NOT GATE	4.223813mw	1.318593mw
NOR GATE	8.866097mw	4.136027mw
2*1 MULTIPLEXER	9.5e-8mw (0.00000095)	7e-9mw (0.000000007)
FULL ADDER (SUM)	19.87048mw	9.86526mw
FULL ADDER (CARRY)		3.046574mw

IV. CONCLUSION AND FUTURE SCOPE

Conclusion

The conclusion that we can draw is that adiabatic circuits dissipates less power than conventional CMOS circuits. Also, Full-adiabatic circuits like SCRL, ECRL go long way towards achieving adiabatic operation. But they make the circuit complex and offers low throughput. In contrast to this Quasi-adiabatic logic styles viz. PFAL, 2N2P, 2N-2N2P, and PAL which use cross coupled PMOS transistors are more practical circuits as these reduce the complexity of the circuit at the cost of little non-adiabatic loss. Hence, it is concluded that there is a possibility of improving the performance of such quasi-adiabatic circuits, in terms of energy dissipation, by using different circuit techniques.

From the above observation, it can be also be concluded that PFAL technique is energy efficient as compared to Conventional or traditional technique. The power dissipation is greatly reduced due to recycling process in PFAL. When compared with the previous year results the power results are reduced with the decrease in technology used.

Future Scope

In future, researchers can design other logic circuits like demultiplxer, shift register etc or the same circuits with different technology. Adiabatic technology can also be used in development of space crafts, adiamems and nano technology in the near future.

Adiabatic logic is a potential successor for static cmos circuit design when it comes to ultra-low-power energy consumption. Future development like the evolutionary shrinking of the minimum feature size as well as revolutionary novel transistor concepts will change the gate level savings gained by adiabatic logic. In addition, the impact of worsening degradation effects has to be considered in the design of adiabatic circuits. The impact of the technology trends on the figures of merit of adiabatic logic, energy saving potential and optimum operating frequency, are investigated, as well as degradation related issues. Adiabatic logic benefits from future devices, is not susceptible to hot carrier injection, and shows less impact of bias temperature instability than static CMOS circuits. Major interest also lies on the efficient generation of the applied power-clock signal. This oscillating power supply can be used to save energy in short idle times by disconnecting circuits.

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