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Design of High Speed Multiplier Using Vedic Mathematics Technique

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Abstract–

Now-a-days everybody wants high speed processor which may take less time for execution. Due to its high speed processing ability, a multiplier is needed. The mostly occurring problems in a multiplier are power dissipation and more delay. So we use Vedic multiplier which results in minimum delay. We are using 4x4 bit Vedic Multiplier which consists vertical and crosswise algorithm. This process has been seem to be large optimization of speed. We made this project with the help of Xilinx software.

Keywords- Vedic multiplication, Half Adder, Full Adder, VHDL, hardware design.

I. INTRODUCTION

In earlier days, the speed is our main motive and. In advanced technology multiplier fulfill the requirement of speed. Multiplier performs the multiplication which is an important fundamental function of arithmetic operation. Multiplier is used in the digital signal processing for fast calculation that is required time is less to perform the operation.

The Vedic mathematics was rediscovered from 1911 to 1980 by Shri Bharti Krishna Tirthaji. This technique contains 16 sutras and in this paper we will study the architecture which is based on Urdhava Triyakbhyam. In this technique vertically and crosswise operation is performed according to sutras. In this paper the basic logic for 4x4 multiplier is implemented having less hardware is used. This technique having different application areas in engineering technology until booths and array algorithms are successful.

Digital multipliers are rarely used component in digital circuit design the component used in digital circuit design is fast and efficient components used for implementation. There are various types of multipliers available selection of the multiplier is based upon the arrangement of the module.

As need of high speed processors increasing the need of high speed multiplier is also increasing. Multiplier is one of the key hardware blocks in most fast processing systems which is not only a high delay but also a major source of power dissipation. To overcome this problem we use 4×4 bit Vedic mathematics techniques in multiplier.

II. VEDIC MULTIPLICATION

Our project on Vedic Multiplier is based on ”Urdhva Tiryakbhyam” Sutra (algorithm).In decimal number system, these sutra is mostly used for multiplication process. In our work, we use the same technique for binary number system so that the processing algorithm must be compatible with the digital hardware. Its casual multiplication formula could be applicable to all the cases of multiplication process. It means vertical and crosswise algorithm of multiplication. It is based on basic concept through which the execution of partial products can be done. The Vedic Multiplier consists of 4 inputs, and we get its resultant output of 8 bits. If the input is of maximum n-numbers then its resultant output is of maximum 2n-bits by multiplication. A3, A2, A1, A0 and B3, B2, B1, B0 are the two inputs taken in 4x4 Vedic multiplier.

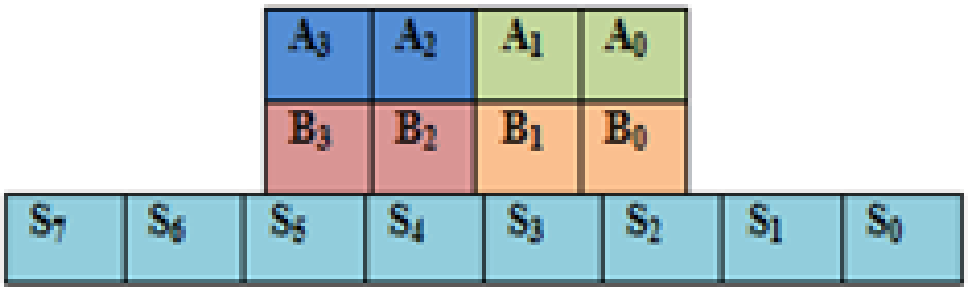

Fig. 1: 4-bit Vedic Multiplier

THE VEDIC SUTRAS WITH THEIR MEANINGS ARE LISTED BELOW:
There are 16 Vedic sutras which are listed below with their meanings.

1. (Anurupye) Shunyamanyat –One of them is in ratio then other value is in ratio.
2. ChalanaKalanabyham -Differences and Similarities
3. EkadhikinaPurvena- The value is more than the previous one.
4. EkanyunenaPurvena –The value is less than the previous one.
5. Gunakasamuchyah-The factors of sum is equal to sum of factor.
6. Gunitasamuchyah-the product of sum is equal to sum of product.
7. NikhilamNavatashcaramamDashatah -The value from 9 and last from 10.
8. ParaavartyaYojayet-Transpose and adjust the values.
9. Puranapuranabyham - completion or noncompletion.
10. Sankalana- vyavakalanabhyam -By addition and by subtraction.
11. ShesanyankenaCharamena- The remainders by the last digit.
12. ShunyamSaamyasamuccaye -When the sum is equal then its sum is zero.
13. Sopaantyadvayamantyam -The ultimate and twice the penultimate.
14. Urdhva-tiryakbhyam -It performs vertically and crosswise operations.
15. Vyashtisamanstih -Part and Whole.
16. Yaavadunam- Whatever the extent of its deficiency.

This all are the 16 Vedic sutras. The Vedic multiplication technique is based on one of the sutra named as "Urdhva Tiryakbhyam". The vertical product of bit A0 & B0 gives the output S0.The sum A0.B0 &A1.B0 gives the output S1 which is 10 bit of its previous sum S0.And the remaining multiplication is done with same method. The position of ten's and hundred bits are forward carry to the next addition performed. From the 10's bit S6 the answer of S7 bit will come in the multiplication process. The multiplication process is shown in figure with different architectures.

III. URDHVA TIRYAKBHYAM SUTRA

For n x n bit number, "Urdhva Tiryakbhyam" (vertical and crosswise) algorithm can be generalized. The Vedic multiplier has advantage that as the number increases, delay and the area increases very slightly as compared to other multipliers. It is very important that the multiplier must have great speed with minimum delay. This architecture is generalized in the terms of silicon area and speed. Since the partial product, the multiplier has high advantage that the number and their sum are calculated in parallel and crosswise method. By referring the Vedic Multiplier, due to its structure, it can be easily layout in microprocessors and designs can easily adopted the power of multiplier. It can easily increases by increasing the input and output data bus area, since it has a consistent problems to avoid device failure. The main advantage is that it decreases the need of microprocessor to operate at high clock frequency pulses. It generally results in increased processing power when at higher clock frequency. The power dissipation increases which result in higher device operating temperature, is noted as the only disadvantage.

IV. ADDER STRUCTURE

In this paper, we use 4-bit Full Adder to implement the Vedic Multiplier.
4-bit Full Adder – Carry in and carry out chains together are consisted by a 4-bit Full Adder, where the carry bit ripples from 1 bit to the next bit. All four Full Adders are internally connected to other Adders, whereas each full adder supplied with two individual inputs.

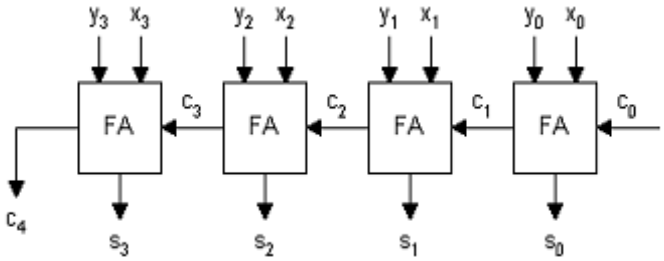

Fig.2: 4-bit Full Adder

The two Boolean functions for the sum and carry are:
SUM = Ai ⊕ Bi ⊕ Ci
Cout = Ci+1 = Ai · Bi + (Ai ⊕Bi) · Ci

V. BLOCK IMPLEMENTATION OF 4X4 VEDIC MULTIPLIER

The block implementation by using "Urdhva Tiryakbhyam" sutra of 4x4 Vedic Multiplier is shown in the fig-4. The 4x4 Multiplier is assembled by using four 2x2 Vedic multipliers, two 4-bit Full Adders and one Half Adder. Each 2x2 Vedic Multiplier consists of two individual inputs which are internally connected. For the design of 4x4 blocks, the first step is to make a group of two bit of each 4-bit input. This two bit of 4-bit group will result in the formation of vertical and crosswise product. The vertical and crosswise is shown by the partial product.

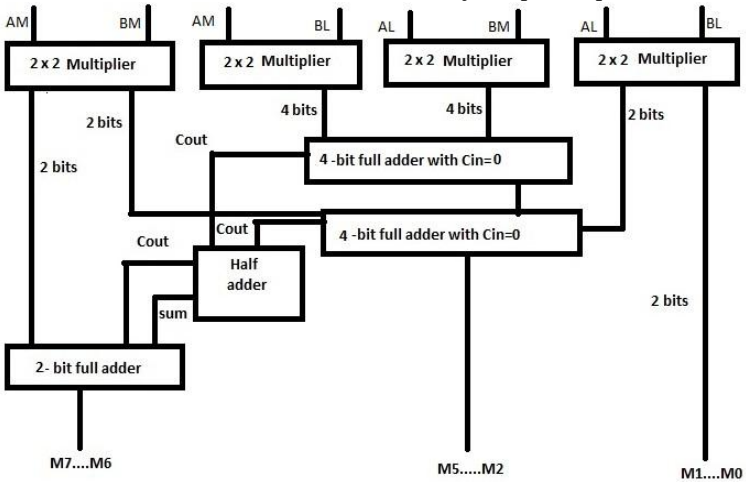

Fig.3. Block Diagram of 4-bit Vedic Multiplier with 4-bit Full Adder

VI. SIMULATION OF 4X4 MULTIPLIER

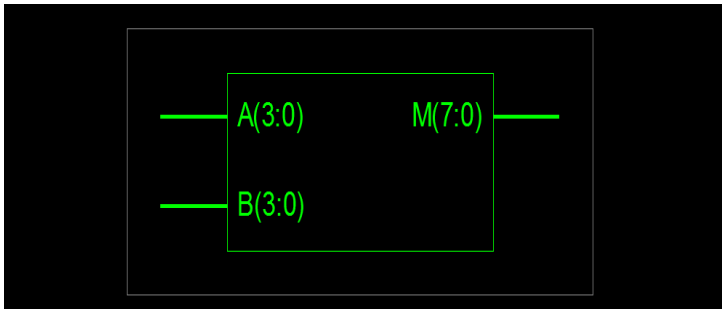

Fig.4: Block view of 4-bit Vedic Multiplier

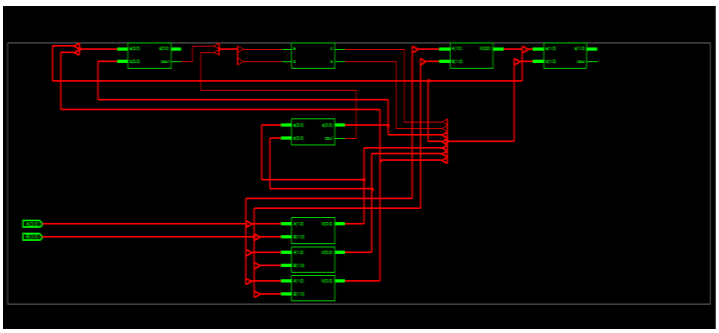

Fig.5: RTL view 4-bit Vedic Multiplier

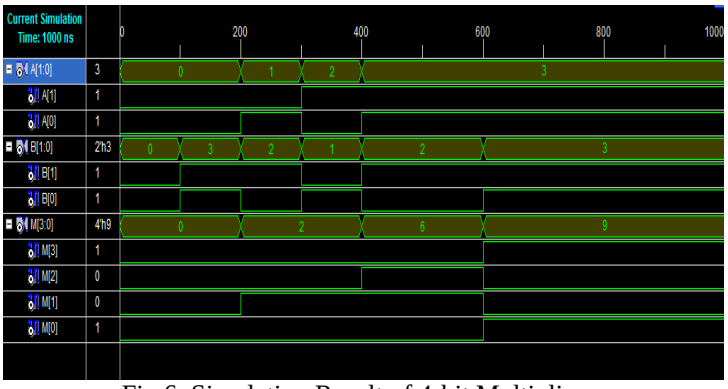

Fig.6: Simulation Result of 4-bit Multiplier

VII. RESULT ANALYSIS

Table 1: Comparison of Multiplier in the terms of delays

Types of multiplier (4 bit)	Delay(ns)
Vedic Multiplier with Ripple Carry Adder	15.32 ns
Traditional Booth Multiplier	24.03ns

The above table gives us comparison between Vedic Multiplier with A traditional Booth Multiplier. The coding of 4x4 Vedic multiplier is done in VHDL. It is simulated by using Xilinx ISE14.2.Software.
The above result shows that Vedic Multiplier with Ripple Carry Adder is fast as compared to the Booth and Array Multiplier. It is much better than the other multiplier in terms of speed and delay.

VIII. CONCLUSION

The Vedic multiplier has been design for the purpose of high speed processing and less delay. Array and Booth multiplier are not effective as compared to Vedic multiplier. Hence Urdhava Tiryakbhyam multiplier is considered as the best multiplier in terms of speed and delays.

ACKNOWLEDGEMENT

"It is said that the road to success begins with just a step in the right direction. What are required are the urge to excel and the ability to work hard consistently. Proper application of knowledge and expert guidance are essential ingredients of success". The project work titled **"**Design of High Speed Vedic Multiplier Using Vedic Mathematics**"** being submitted will remain incomplete unless we thank all those who helped us directly and indirectly for the successful completion of this project.

REFERENCES

[1] Jagadguru Swami, Sri Bharati Krisna, Tirthaji Maharaja, "Vedic Mathematics or Sixteen Simple Mathematical Formulae from the Veda, Delhi (1965)", Motilal Banarsidas, Varanasi, India, 1986.
[2] Pushpalata Verma, K. K. Mehta International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-1, Issue-5, June 2012
[3] H. Thapliyal and H.R Arbania. "A Time-Area-Power Efficient Multiplier and Square Architecture Based On Ancient Indian Vedic Mathematics", Proceedings of the 2004 International Conference on VLSI (VLSI'04), Las Vegas, Nevada, June 2004, pp. 434-439.
[4] Thapliyal H. and Srinivas M.B, "High Speed Efficient NxN Bit Parallel Hierarchical Overlay Multiplier Architecture Based on Ancient Indian Vedic Mathematics", Transactions on Engineering
[5] P. D. Chidgupkar and M. T. Karad, "The Implementation of Vedic Algorithms in Digital Signal Processing", Global J. of Engg. Edu, Vol.8, No.2, 2004, UICEE Published in Australia
[6] Thapliyal H. and Srinivas M.B, "High Speed Efficient NxN Bit Parallel Hierarchical Overlay Multiplier Architecture Based on Ancient Indian Vedic Mathematics", Transactions on Engineering, Computing and Technology, 2004, Vol.2.
[7] Harpreet Singh Dhillon and Abhijit Mitra, "A Reduced– Bit Multipliction Algorithm for Digital Arithmetics", International Journal of Computational and Mathematical Sciences 2.2 @ www.waset.orgSpring2008.
[8] Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim and Yong Beom Cho, "Multiplier design based on ancient Indian Vedic Mathematician", International SoC Design Conference, pp. 65- 68, 2008.

