International Journal of
Emerging Research in Management &Technology
ISSN: 2278-9359 (Volume-4, Issue-2)

Research Article | **February 2015**

Reed-Solomon Error Correction

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Abstract-

The main aim of this paper is to give some essential background to the theory of Reed Solomon codes and the previous survey literature of the Reed Solomon error correction method using various algorithm.Reed Solomon codes have shown to be the best compromise between efficiency and complexity. These are cyclic codes and are used for the detection and correction of burst errors. Galois field is used for encoding and decoding of reed Solomon codes.

Keywords: FPGA, Galois Field arithmatic, RS Code, BCH Code,CR Code.

I. INTRODUCTION

1.1 OVERVIEW

Reed-Solomon Codes are error-correcting linear cyclic systematic non-binary block 8 code.This codes range from data retrieval from bar codes and QR codes in our daily lives for sending transmissions to and from spacecrafts launched in deep-space missions. The Reed-Solomon (RS) Code was discovered by Irving Reed and Gus Solomon. Since then, RS Codes have been an huge contributor to the telecommunications revolution in the last half of the twentieth century. Reed-Solomon codes are the most frequently used digital error control codes they are used in computer memory and non-volaitile memory applications.Some of the applications include the Digital Audio Disk, Deep Space Telecommunication Systems, Error Control for Systems with Feedback, Spread-Spectrum Systems, and Computer Memory.RS codes are generated and corrected using Reed-Solomon encoder and decoderIn the encoder Redundant symbols are generated using a generator polynomial and appended to the message symbols. In decoder error location and magnitude are calculated using the same generator polynomial. Then the correction is applied on the received code.Reed Solomon code has less coding gain as compared to LDPC and turbo codes. But it has very high coding rate and low complexity. Hence it is suitable for many applications including storage and transmission.

II. LITERATURE SURVEY

2.1 SUMMARY OF PREVIOUS PAPERS

This chapter represents an overview of background research to the project. The literature also gives the brief idea about the technical, operational and economical feasibility study.

a. Kenny Chung Chung Wai, Dr. Shanchieh Jay Yang" Field Programmable Gate Array Implementation of Reed-Solomon Code, RS(255,239)"In proceeding of 9th Annual Military and Aerospace programmable logic Device International Conference,2 september 2011.

Authors Kenny Chung Chung Wai, Dr. Shanchieh Jay Yang introduced a FPGA implementation of Reed Solomon. It is synthesized to Altera's Stratix II and benchmarks are run against Altera's Reed Solomon code. Author was designed Xelic's encoder which is measured to be about half the size of Altera's encoder.[1]

b. Joaquin Garcia, Rene Cumplido Department of Computer Science , "On the design of an FPGA-Based OFDM modulator for IEEE 802.16-2004" INAOE, Puebla, Mexico 2005

Author Joaquin Garcia introduced OFDM using System generator and Matlab & Simulink.The results on hand show that it is possible to implement an OFDM modulator for IEEE Std.802.16 using Virtex II. In this paper the author implement configurable system that can be implemented for different modulation technique. The future work of this paper is Implementation of the FEC modulator, demodulator. [3]

c. K. Harikrishna, T. Rama Rao, and Vladimir A. Labay, "FPGA Implementation of FFT Algorithm for OFDM Based IEEE 802.16d (Fixed WiMAX) Communications" Journal Of Electronic Science And Technology, Vol. 8, No. 3,September 2010

Authors K. Harikrishna, T. Rama Rao, and Vladimir A. Labay, introduced a high level implementation of a high performance FFT for OFDM modulator and demodulator of 802.16d. The design has been coded in Verilog and besieged into Xilinx Spartan3 field programmable gate arrays. The design of the FFT is implemented and applied to fix WiMAX—IEEE 802.16d communication standard. [4]10

d. Miljko Bobrek, Kenyon H. Clark, Austin P. Albright "FPGA Implementation of Reed- Solomon Decoder for IEEE 802.16 WiMAX Systems using Simulink-Sysgen Design Environment" Oak Ridge National Laboratory Cognitive Radio Program 1 Bethel Valley Rd Oak Ridge ,TN 37831.

Authors Miljko Bobrek, Kenyon H. Clark, Austin P. Albright introduced FPGA implementation of the Reed- Solomon decoder for used in IEEE 802.16 WiMAX systems.The decoder is based on RS (255,239) code. It is additionally shortened and punctured according to the WiMAX specifications. A Simulink model was used for simulation and hardware implementation. It is based on the System Generator library of low-level Xilinx blocks [6]

e. M.A. Mohamed, A.S. Samarah, M.I. Fath Allah , "Implementation of the OFDM Physical Layer Using FPGA" IJCSI International Journal of Computer Science Issues,Vol. 9, Issue 2, Nov2, March 2012

Author M.A. Mohamed, A.S. Samarah, M.I. Fath Allah introduced the design and implementation of OFDM system. Author has tested system performance by considering various design parameters using MATLAB 2011. All modules are coded using VHDL programming language.[7]

f. Yuval Cassuto, Jehoshua Bruck,Robert J.McEliece "On the Average Complexity of Reed–Solomon List Decoders" IEEE Vol. 59, No. 4, April 2013.

Authors Yuval Cassuto, Jehoshua Bruck,Robert J.McEliece**,** introduced the number of monomials required to interrupt a received word in an algebraic list decoder for Reed–Solomon codes depends on the instantaneous channel error. On the basis of logical side, this paper studies the dependence of interpolation costs on instantaneous errors, in both hard- and soft-decision decoders.[8]

g. Li Chen et.al. "Progressive Algebraic Soft-Decision Decoding of Reed-Solomon Codes" IEEE Vol. 61, No. 2, February 2013

Author Li Chen, introduced algebraic soft-decision decoding (ASD) algorithm. They are a polynomial-time soft decoding algorithm for Reed- Solomon (RS) codes. It breaks both the 11 algebraic hard decision decoding (AHD) and the conventional unique decoding algorithms;

this paper proposes a progressive ASD (PASD) algorithm that enables the conventional ASD algorithm to perform decoding with an adjustable designed factorization output list size (OLS).[9]

h. F. Abdelkefi, J. Ayadi "Reed-Solomon code-based sparse channel estimation for OFDM systems" IEEE Vol. 48 27th September 2012.

Authors F. Abdelkefi, J. Ayadi, introduced a novel efficient algorithm for the opinion of sparse channel impulse response (CIR) is addressed for OFDM systems. The innovation of this algorithm comes from the fact that it equivalently see the CIR estimation problem as a decoding one. To do so, it uses first the channel sparsely through the modeling of the sparse CIR as a Bernoulli-Gaussian process. Then, using the relationship between the Reed-Solomon codes and the OFDM modulator it efficiently estimates the sparse CIR using

directly the decoding of the OFDM received signal. The obtain simulation results highlight that using the planned algorithm gives good estimation performance in terms of mean squares error on the sparse CIR estimates. Which concludes that using a multicarrier OFDM

transmission system, pilot tones can be seen as virtual RS code words. [10]

i. Li Li et. al. "Unified Architecture for Reed-Solomon Decoder Combined With Burst-Error Correction" IEEE Vol. 20, No. 7, July 2012.

Author Li Li, introduced Reed-Solomon (RS) codes. These codes are widely used as forward correction codes (FEC) in digital communication and storage systems. Correcting errors of RS codes have been extensively calculated in both academia and industry. However, for burst-error correction, the research is still limited due to its ultra-high computation complexity. Then, based on the planned algorithm, a unified VLSI architecture that is capable of correcting burst errors, as well as random errors and erasures, is firstly presented for multimode decoding requirements.[11]

j. Xinmiao Zhang, Yu Zheng "Systematically Re-encoded Algebraic Soft-Decision Reed–Solomon Decoder" IEEE Vol. 59, No. 6, June 2012.

Authors Xinmiao Zhang, Yu Zheng, introduced a model to reduce the complexity of algebraic soft-decision decoding (ASD) of Reed–Solomon (RS) codes; re-encoding and 12 coordinate transformation can be applied. For an (n, k) code, the re-encoding was implemented as applying erasure decoding to the k most reliable code positions previously.Such re-encoding can occupy a significant part of the overall decoder are. As a result, the proposed decoder can achieve much higher efficiency than prior designs. Our future work will exploit if systematic re-encoding can be employed in general ASD decoders. [12]

k. J.-I. Park, H. Lee "Area-efficient truncated Berlekamp-Massey architecture for Reed Solomon decoder" 17th February 2011.

Authors, J.-I. Park, H. Lee, introduced a new area-efficient truncated inversion less Berlekamp-Massey architecture for the Reed-Solomon (RS) decoder, where RS decoder is one of the forward error correction techniques. The area-efficient feature of the proposed architecture is obtained by truncating redundant processing elements in the key equation solver

(KES) block using the BM algorithm. This enhances the hardware utilization of the processing elements used to solve the key equation and reduces the hardware complication of the KES block. [13]

l. Christian scholar, "Code Generation Tools for Hardware Implementation of FEC circuits", http://www.fous.gmd.de/research/cc/mobis/publ/doc/1999/code_gen.pdf.
Author Christian scholar introduced VHDL code generator for Reed-Solomon decoders using Euclid's algorithm. The VHDL code is synthesizable, and area and speed metrics for several decoder designs is presented, targeted to Xilinx Field Programmable Gate Arrays. The core generator also generates the vectors for the test bench. The code generator is capable of generating VHDL code for most binary FEC decoder, such as Hamming, Cyclical Redundancy Check (CRC), and BCH codes. In the design of the Reed-Solomon decoder, a bank of Galois multipliers is used, as opposed to a dedicated multiplier where it is needed.This result is less area, but requires tristate buses and reliable scheduling of the steps to avoid collisions.[30]

m. Jong Kang Park And Jong Tae Kim, " A Soft IP Compiler For Reed-Solomon Decoder", http://www.sipac.org/ap-soc/index_k/index_a/source/A04_lec.pdf.
Author Jong Kang Park And Jong Tae Kim introduced a program that generates synthesizable VHDL code for Reed-Solomon decoder is presented. Erasure decoding is supported. The method of solving the key equation is the inversion less Massey-Berlekamp algorithm, or a modified version called the reformulated inversion less Massey-Berlekamp algorithm. The choice of the algorithm is user controlled. The area and speed metrics are provided for several designs. The average throughput achieved is 500Mbits/second in ASIC.This is comparable to the results achieved by the code generator of the thesis when applied to Xilinx FPGAs.[31]

III. CONCLUSION OF LITERATURE SURVEY

In the area of Reed-Solomon codes Christian scholar has implemented code generator for Reed-Solomon Decoder using Euclid's algorithm. The code generator is capable of generating VHDL code for most binary FEC decoder, such as Hamming, Cyclical
Redundancy Check (CRC), and BCH codes. In the design of the Reed-Solomon decoder, a bank of Galois multipliers is used, as opposed to a dedicated multiplier where it is needed.Jong Kang Park and Jong Tae Kim implemented inversion less Massey-Berlekamp algorithm for Reed-Solomon Decoder on ASIC. Xinmiao Zhang, Yu Zheng, introduced a model to reduce the complexity of algebraic soft-decision decoding (ASD) of Reed–Solomon (RS) codes; re-encoding and coordinate transformation can be applied. For an (n, k) code, the reencoding
was implemented as applying erasure decoding to the k most reliable code positions previously. Such re-encoding can occupy a significant part of the overall decoder are. As a result, the proposed decoder can achieve much higher efficiency than prior designs. J.-I. Park
and H. Lee presented a new area-efficient truncated inversion less Berlekamp-Massey architecture for the Reed-Solomon (RS) decoder, where RS decoder is one of the forward error correction techniques. The area-efficient feature of the proposed architecture is obtained by truncating redundant processing elements in the key equation solver (KES) block using\the BM algorithm. This enhances the hardware utilization of the processing elements used to solve the key equation and reduces the hardware complication of the KES block.

IV. PROBLEM STATEMENT

It has been noticed that the present Reed-Solomon Decoder are very large in area and their speed is not too fast. Since Galois field inverters are very complex, several times more so than a Galois field multiplier, a key solver that eliminates the need for such an inverter can yield savings in decoder latency. Such an algorithm is the inversionless massey-berlekamp algorithm by Reed, Shih and Truong [6]. However, the drawback to this algorithm is that it only computes the error – locator polynomial.In the inversionless massey-berlekamp algorithm, the error- evaluator polynomial is computed then by multiplying the error – locator polynomial by the syndrome polynomial. This results in extra latency of the order of the error-locator polynomial, and as a result an extra number of gates and registers are needed.

V. PROPOSED WORK

In this paper, the extended inversion less Massey-Berlekamp algorithm is used. The extended inversion less Massey-Berlekamp algorithm overcomes the extra latency by computing both the error - locator polynomial and the error – evaluator polynomial at the same time. In this thesis, (255,239) reed Solomon codes have been designed and implement using Spartan field programmable gate array device. The design is carried out by writing VHDL code. The waveforms are tested using the package ISIM simulator and synthesis report and programming file are obtained using the Spartan 6.

ACKNOWLEDGMENT

It is my pleasure and privilege to acknowledge and express my deep sense to my guide Prof. Ravikant sharma for his contribution to this work.

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