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Prerequisites of RF CMOS Devices at High Frequency and the Related Design Issues

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Abstract—

Personal computers and multimedia equipments demand high throughput and broad band wireless communications. The thirst for designing RF circuits to push the devices to operate at high frequency keeps growing. Design issues and modelling methodology of RF CMOS device to operate at high frequencies are discussed. Difficulties faced by current CMOS models and its lack of accuracy in capturing high frequency are focused. To improve model accuracy, Vendor modelling approach is discussed to model frequency dependent parameters like substrate resistance, gate resistance and noise signals. In this connection, few design techniques of RF CMOS device to improve frequency dependent parameters are discussed. Limits possessed on CMOS scaling and an insight into the next generation CMOS devices have been overviewed.

Keywords— RF, CMOS, gate resistance, multigate MOSFETs, high frequency

I. INTRODUCTION

Radio frequency (RF) technologies serve the rapidly growing advanced communications and "More-than-Moore (MtM)" markets and represent essential and critical technologies for the success of many semiconductor manufacturers and the ultimate success of the future Internet of Things (IoT). Communications products and emerging products that support applications such as radar imaging, defence, and homeland security all have functionalities enabled by MtM, RF, and AMS technologies. RF technology is becoming one of the key drivers for high volume manufacturing. Consumer products account for over half of the demand for semiconductors. Fourth generation (4G) cellular phones and tablets now have a much higher RF and AMS semiconductor content and now are a very large fraction of the mobile market compared to only 5 % of the market a few years ago. The iPad for example has more than 19 RF and AMS front-end components. The physical realization of RF IC (Radio Frequency Integrated Circuit) design using CMOS devices offers several advantages including low cost, high integration, high noise immunity, low static power consumption and easy access to the technology [1]. But CMOS devices suffer from heavy substrate loss which has led to the development of GaAs and InP based devices. But still CMOS devices are preferred due to wide scaling possibilities which makes the device suitable for high frequency application by increasing transition frequency, ft.

A. Requirements of RF CMOS Device.

The continuous scaling of CMOS has made this technology a candidate for RF applications. CMOS technology is attractive because of low cost, high integration and easy access to the technology. The primary requirement of RF CMOS device is that it should have lower channel length (L) and wider channel width (W). These make the device current to increase (1) which further increases *ft* (2) and Unity power gain frequency, *fmax* (3). The drain current in saturation neglecting channel length modulation is given by

$I_D = k\,(W/L)\,(V_{GS} - V_t)^2$ ------- (1)

$ft \;\alpha\; (1/L^2)$ ---------- (2)

where k' = process transconductance (A/V^2);

V_{GS}=Gate Voltage (V); V_t = Threshold Voltage (V);

$fmax \;\alpha\; (Rout/R_G)^{1/2}$----------(3)

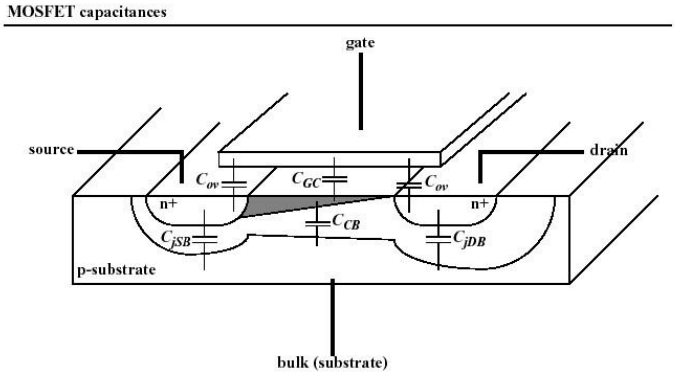

Fig. 1 Junction Capacitances of MOSFET

Therefore it is evident from equation (2) and (3) that *fmax* can be improved by increasing Rout , the output resistance of the device with respect to the substrate and by decreasing the gate resistance RG of CMOS device [2]. High Rout means increasing the substrate resistance from source to bulk and from drain to bulk. Normally reverse biased junction capacitances *Csb* & *Cdb*, as shown in Figure 1 ensure that there is a high resistance between active region and bulk.

Lower gate resistance drives the MOSFET in high frequency operation and also it offers low delay to the input side of the MOSFET. Considering these, the paper discusses glitches in designing RF IC design and its related issues.

II. RF IC DESIGN

Each and every component of RF IC circuit has to be optimized to fit into RF frequency regime because in RF and millimetre frequency range, each section of semiconductor has distributed parasitic. This is the main difference between RF IC design and Digital IC design. This especially holds for active devices like CMOS transistor as they are the core device involved in amplification.

A. Issues in RF CMOS Device Modelling

Circuit engineers rely on circuit simulators for verification of their design before fabrication. Circuit simulators, in turn depend on device models to generate and construct circuits. Issues related to MOSFET models that are commonly used in circuit simulators are discussed. It is found that there is always some sort of divergence existing between the simulated output and the fabricated one (which is called the measured data). The reason for this discrepancy is that the core models used in the circuit simulator describe the behaviour of devices operated in DC and low frequency regime. In real time, devices exhibit additional parasitics in all its terminals say, source, drain, gate and substrate resistances, capacitances and inductance effect due to high frequency signal given to it. These effects are not captured by the available MOS models [3]. Also, each section of the device has to be treated as transmission line model at RF regime which is again frequency dependent. A few popular MOSFET models which lag behind the description of high frequency parasitics are listed in the Table 1.

TABLE I A SHORT COPMARISON OF VARIOUS DEVICE MODELS

Parameter	**BSIM3**	**MOS Model9**	**BSIM4**	**MOS Model 11**
Source and Drain Series Resistance	RS & RD are included in IDC, so inaccuracy at HF			
Non-Quasi Static Model	NQS @ HF	No	NQS @ HF (with r_i)	NQS added using channel segmentation
Short Channel Effect	Includes SCE	No		
Gate and Substrate Resistance	No	No	Included	Included

B. Supplier Modelling Approach

Recent device models are based on semi empirical analytical modelling. This consists of a set of equations that are solved by assigning the parameters. The model parameters are those values that are determined by experimental results. Parameters like process transconductance, body bias coefficient etc. are obtained from experimental results whereas high frequency related parasitic are not determined or computed in the model file. This is the deficient aspect in current model files and if they are used in simulation of RF circuit design then the simulated results would deviate from the measured results due to the inaccuracy of model files. So, many researchers worked on determining the gate and substrate resistance and it paved way to Vendor/Supplier modelling approach [4].

Based on circuit designer's demand, certain vendors started working on the exploration of high frequency parasitics and included them in the core model. Figure 2 clearly differentiates the mainstream core with its related parasitics. Following this supplier modelling approach, one could increase the accuracy of the existing device models.

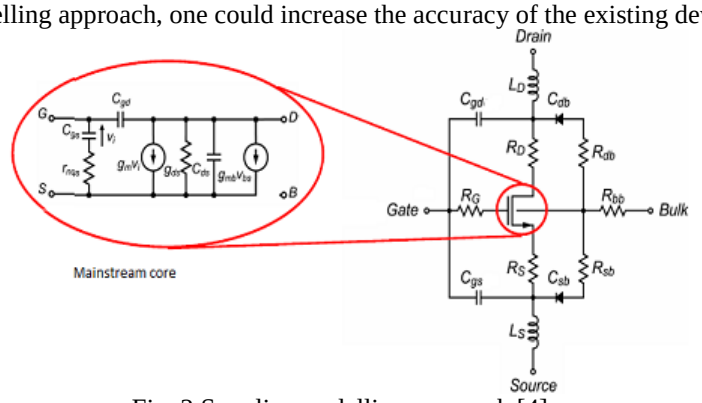

Fig. 2 Supplier modelling approach [4]

C. Substrate Resistance Modelling

Among the parasitics listed, substrate resistance and gate resistance are important as they determine the upper operating frequency of a device, given by equation (2) and (3). As these resistances are frequency dependent, device

models should mandatorily update these resistances for its accuracy. A small signal MOSFET model is depicted in Figure 3. Treating it as a two port network, y-parameters are derived as follows.

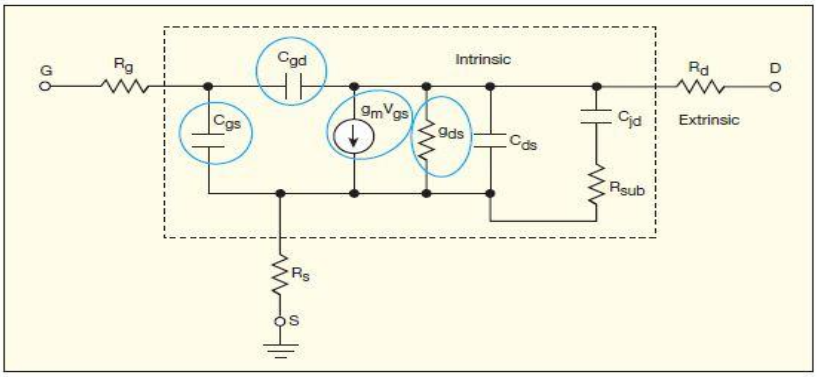

Fig. 3 The small signal equivalent circuit of CMOS device

The substrate resistance [5] can be calculated using

$Rsx = Real\ (Y_{22}) / (img(Y_{22} + Y_{12}))^{2}$ ---------- (4)

Equation (4) indicates clearly that substrate resistance depends on frequency and it adversely affects the device performance if the device is subjected to RF frequency signal and millimetre wave signal. The current models do not capture this degradation. Similarly, the gate resistance also changes due to increase in signal frequency.

Paper [6] indicates that modern ICs suffer from resistive and capacitive coupling of interconnects with the substrate causing noise. This work is focused on modelling the distributed effects of a large interconnect parallel to substrate using the 3D boundary element method. This approach has a drawback that it is difficult to find noise injection areas and/or noise picking areas.

Another approach describes a physically based model for substrate resistance [7]. Because of the multifingered layout, the device sees multiple unequal paths through the substrate to the ground. The resulting network is computationally complex, so the authors have proposed to reduce this to few lumped resistances. That is, the path through the substrate is divided into two; one through the active area and the other is under the shallow trench isolation (STI).

Next, the design of scalable model of substrate resistance components for RF MOSFETs using bar type body contact set in horizontal direction to gate poly is attempted [8]. The model equations for substrate resistances based on number of fingers (*Nf*) for bar type body contacts are derived. The designed model is scalable not only for *L*, *Nf* and *Wf* but also for various layout dimensions, such as body-contact to active region distance and gate poly to gate poly distance.

Next the impact of substrate contact ring shape and its placement on the substrate are studied in [5]. Structures of varying shape of gate finger, substrate ring and the variation of substrate ring position relative to the device are fabricated and measured data of substrate resistance, *ft* and *fmax* are obtained pertaining to 45 nm CMOS devices.

D. Gate Resistance Modelling

It is found in the literature that RG also influences the performance of RF CMOS device. A physics-based effective gate resistance model [9] representing the non-quasi-static (NQS) effect and the distributed gate electrode resistance using 2-D simulations and extracted values are verified with experimental (measured) data. In addition, the effect of the gate resistance on the device noise behaviour has been studied.

Another approach deals with the characterisation of gate resistance of MOSFETs for various geometries [10] working at various bias conditions at high frequency (HF). Variation in the gate resistance with channel length and/or per finger width upto a critical dimension of *Lf* or *Wf* is presented. The results were based on measurements.

E. Modelling of Noise Sources

It is known that thermal noise prominently dominates in RF CMOS devices. So studies reveals that the drain channel noise, gate resistance noise and induced gate current noise are the common thermally generated noise sources that are to be computed [2] and included in the small signal equivalent circuit representation.

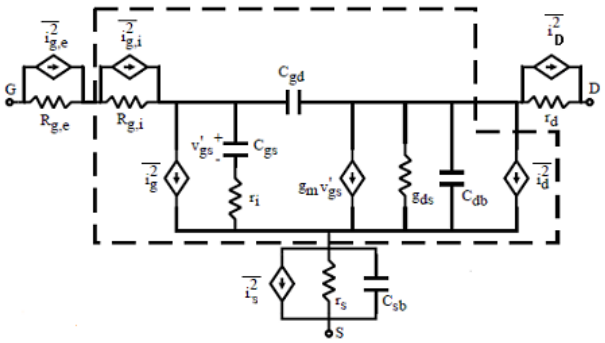

Fig.4 A complete small signal representation of RF CMOS device [2]

The noise sources occur in RF CMOS devices are thermal in origin. The generalised expression of noise sources that are generated at the terminals of CMOS device is given by

$\hat{I}_x^2 = (4kT\Delta f)/ Rx$ ---------- (5)

Where *Rx* = resistances at the terminals of MOS (Gate, Source to substrate resistance and Drain respectively)

K = Boltzmann's constant;

T=Temperature in Kelvin;

Δf = Bandwidth;

Generally the resistance at device terminal is divided into internal part (intrinsic or core part) and the external part (terminal resistance). Since the gate is wider, its resistances are subdivided into internal part (due to the distributed resistance at the gate) and the external part (terminal resistance) as shown in Figure 4.

Next prominent noise sources is the drain channel noise which is given by:

$\hat{I}_d^2 = 4kT\gamma g_{do}\Delta f$ ---------- (6)

Where *gdo* = Conductance of the channel at zero V_{DS}. The drain channel noise depends on the conductance of the channel.

And the next source is induced gate noise which is given by

$\hat{I}_g^2 = 4kT\beta g_{do} ri\omega C_{gs}\Delta f$ ---------- (7)

Where γ, β = Bias dependent parameter;

r_i = Channel charging resistance;

Cgs = Gate to Source capacitance

This is the noise current from the channel charging resistance and the distributed carriers in the channel that are capacitively coupled into gate through the gate capacitance. The above equations (5)-(7) show that the small signal noise parameters vary with temperature and frequency dependent resistance.

The above study reveals that the substrate resistance, gate resistance and noise models have been carried out as a lumped element representation. Also the results are verified using measurement based data obtained after fabrication. If they are properly modelled, distributed effects are included into the small signal representation, then the accuracy of resultant model increases.

III. TECHNIQUES FOR THE DESIGN OF RF CMOS

CMOS technology is the most common technology whose concepts and fabrication steps are well analysed. It consists of a set of layers which defines a transistor. The procedural steps are understandable and hence its effect on the device performance can be predicted in advance. This type of modelling a device with respect to its associated fabrication modelling steps is called as 'Simulation-based modelling' whereas if a device is fabricated and its parameters are measured by conducting suitable experiments using measuring equipment, it is called 'Measurement-based modelling'.

Simulation-based modelling is simple and cost effective; anyone who has better understanding on device fabrication can follow Simulation-based modelling. This is technology independent, application independent and applicable to any RF circuit. Whereas measurement based modelling approach is expensive as measuring equipment is costly and it is technology based and application based. But in terms of accuracy of parameter, measurement-based modelling scheme offers reliable data, but restricts the flexibility in modelling.

A. Cancellation of Miller's Capacitance

Based on simulation based modelling, paper [11] suggest that layout of transistors connected in differential pair is adjusted so that the negative Miller capacitance is created thus cancelling the Miller effect. This paper also suggests that metallization Capacitances can be extracted in layout level.

B. Multifinger Gate Structure

Since RF CMOS devices demands wider channel width, this increases the resistance of gate material which in turn increases the time delay. This can be mitigated by Multifinger gate structures where the gate is split into number of fingers and this results in reduction of effective gate resistance [12].

C. Increasing the Output Resistance of RF CMOS Device

The output resistance of RF CMOS device can be improved by adjusting the doping profile and channel length. If the doping concentration decreases this may increase the space charge region of reverse biased p-n junction diode of active to bulk region. So *Csb* or *Cdb* decreases thereby its reactance increases (resistance to leakage path).

The layout of CMOS device can be altered to reduce the gate resistance and could increase the output resistance thereby reducing the noise. So layout of a device has strong dependence on its performance [13]. Research has been carried out to add calculated parasitics to the available model resulting in the composite model. Then this model is tested for its accuracy by using in Low Noise Amplifiers[14].

IV. ISSUES IN CMOS DEVICE SCALING

A. Device Scaling Limit

CMOS scaling has allowed the transistor dimensions to be reduced to less than 100nm. As the dimensions shrink, the drain and source regions come closer to each other and their respective potentials interact thus reducing the ability of the gate terminal to control the current flow in the channel. In this connection, few non-linear effects such as Drain Induced

Barrier Lowering (DIBL), body transconductance, velocity saturation, hot carrier effects, sub threshold voltage slope swing, band to band tunnelling, etc. occur thus degrading the device performance. This limits CMOS device scaling.

In order to reduce these non-linear effects, as we scale the channel length, oxide thickness can be reduced and corresponding substrate doping can be increased. These are done to ensure a perfect gate control over the channel. But reduction of oxide thickness causes significant gate current due to direct quantum tunnelling. Similarly increase in the substrate doping causes reduction in carrier mobility and larger junction capacitance [15]-[17].Thus these factors limit further scaling of transistors.

B. Multiple Gate MOSFETs

One of the non-conventional solutions to overcome the nonlinear effects due to scaling is the design of Multiple Gate structure, a new generation CMOS device. A prominent feature of the Multiple Gate MOSFETs is that they do not need heavy channel doping to reduce the non-linear effects. Instead MG MOSFETs use thin body to mitigate the reverse biased p-n junction diodes formed between active and bulk region. Thus leakage paths are controlled and mobility degradation is also avoided. Various structures of Multiple Gate MOSFET have been proposed, such as Double Gate (DG), Surrounding Gate (SG), Triple Gate(TG), Triple Plus Gate(TPG) and Quadruple Gate(QG) as shown in Figure 5.

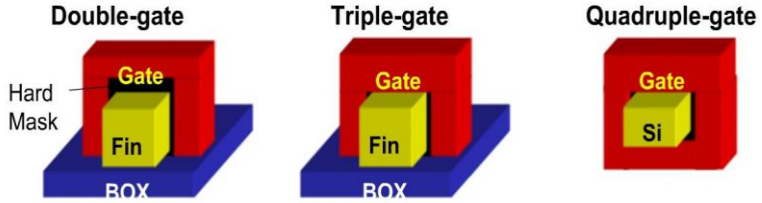

Fig.5 Multiple Gate MOSFETs

Most of the research in constructing RF circuits and microcontrollers are on the line by IC manufacturing companies like AMD, Hitachi, IBM, Infineon Technologies, Intel Corporation, TSMC, University of California, Freescale Semiconductor etc. [18].

V. CONCLUSION

The substrate and gate resistance determine the high frequency characterization of the RF CMOS device. Based on the literature survey, scalable substrate models and gate resistance models suitable for RF and millimetre wave frequency are required and they should be technology and application independent. Their distributed effects are yet to be explored. Along with this, noise models should also be included in the small signal parameters which vary with temperature and frequency dependent resistance. The simulation-based modelling which is flexible and cost effective needs to be explored further to improve the model accuracy.

REFERENCES

[1] Lee, T., H., Wong, S., S. 2000. CMOS RF Integrated Circuits at 5GHz and beyond. In Proceedings of the IEEE, Vol. 88, NO.10, pp.1560-1571.

[2] Golio, J. M. 2001. The RF and microwave handbook. CRC PressI Llc.

[3] Heydari, B., Bohsali, M., Adabi, E., Niknejad, A. M. 2007. Millimeter-wave devices and circuit blocks up to 104 GHz in 90 nm CMOS. Solid-State Circuits, IEEE Journal of, 42(12), 2893-2903.

[4] Saijets, J. 2007. MOSFET RF characterization using bulk and SOI CMOS technologies. VTT Technical Research Centre of Finland.

[5] Gogineni, U., Li, H., Del Alamo, J. A., Sweeney, S. L., Wang, J., & Jagannathan, B. 2010. Effect of substrate contact shape and placement on RF characteristics of 45 nm low power CMOS devices. Solid-State Circuits, IEEE Journal of, 45(5), 998-1006.

[6] Van Genderen, A., van der Meijs, N., & Schrik, E. 2001. Modelling capacitive coupling effects via the substrate. In ProRISC IEEE 12th Annual Workshop on Circuits, Systems and Signal Processing (pp. 366-370).

[7] Chang, R. T., Yang, M. T., Ho, P. P., Wang, Y. J., Chia, Y. T., Liew, B. K., Wong, S. S. 2004. Modelling and optimization of substrate resistance for RFCMOS. Electron Devices, IEEE Transactions on, 51(3), 421-426.

[8] Kang, I. M., Jung, S. J., Choi, T. H., Lee, H. W., Jo, G., Kim, Y. K., Choi, K. M. 2009. Scalable model of substrate resistance components in RF MOSFETs with bar-type body contact considered layout dimensions. Electron Device Letters, IEEE, 30(4), 404-406.

[9] Jin, X., Ou, J. J., Chen, C. H., Liu, W., Deen, M. J., Gray, P. R., Hu, C. 1998. An effective gate resistance model for CMOS RF and noise modelling. In Electron Devices Meeting, 1998. IEDM'98. Technical Digest, International (pp. 961-964). IEEE.

[10] Cheng, Y., & Matloubian, M. 2001. High frequency characterization of gate resistance in RF MOSFETs. Electron Device Letters, IEEE, 22(2), 98-100.

[11] Liang, C., Razavi, B. 2009. Systematic transistor and inductor modelling for millimeter-wave design. Solid State Circuits, IEEE Journal of, 44(2), 450-457.

[12] Razavi, B. 2002. Design of Analog CMOS IntegratedCircuits. Tata Mc Graw-Hill.

[13] Sari. S., Balamurugan, K., Jayakumar. M. 2012. Extraction and Modelling of Metallization Capacitance of MOSFET for Millimeter-wave CMOS Circuits. In Proceedings of ICECT 2012, vol. 3, pp. 538-541.
[14] Sari S., Balamurugan, K., Jayakumar M. 2012. Dependence of Substrate Resistance of RF MOSFET on the Performance of LNA at 60 GHz" IJCSI, vol. 9, no. 4.
[15] George, S., Balamurugan, K., Jayakumar, M. 2012. Analysis of drain current model for multiple gate MOSFETs. In Proceedings of ICETT, vol.2.
[16] Song, J., Yu, B., Yuan, Y., & Taur, Y. 2009. A review on compact modelling of multiple-gate MOSFETs. Circuits and Systems I: Regular Papers, IEEE Transactions on, 56(8), 1858-1869.
[17] Taur, Y., Liang, X., Wang, W., & Lu, H. 2004. A continuous, analytic drain-current model for DG MOSFETs. Electron Device Letters, IEEE, 25(2), 107-109.
[18] www.newsroom.intel.com

