International Journal of

Emerging Research in Management &Technology

Research Article | **May 2014**

Power Efficient on DC-DC Converter Using Filter

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Abstract –

An active filter-based on-chip DC–DC voltage converter for application to distributed on-chip power supplies in multi voltage systems is described in this paper. The performance of an active filter depends strongly on the Op Amp. The gain–bandwidth product of the Op Amp determines the bandwidth of the active filter. Most of the power loss takes place within the Op Amp structure, since the current provided to the output load is supplied by the Op Amp output stage. Hence, the Op Amp needs to provide tens of milliamps of current to the load devices while maintaining sufficient performance to reliably operate the active filter. This project is to evaluate a low power, in ring oscillator modification. The proposed circuit is an alternative to ring oscillator, providing a means for distributing multiple local power supplies across an integrated circuit while maintaining high current efficiency and fast response time within a small area.

Key words - DC-DC converter, Active filter, OP Amp, voltage converter, Ring oscillator

I. Introduction

Very Large Scale Integration is a method of putting the functionality of many different types of electronic components into a small space or chip. This method essentially:

1. Reduces the size of the device.
2. Reduces the cost of the device.
3. Reduces the current consumption.
4. Increases the speed of operation.
5. Offers lots of employments.

With the increasing demand for battery-operated portable applications such as cell phones, PDAs and laptop computers, as well as low-intensity applications such as distributed sensor networks, the need for power sensitive design has grown significantly. It has been shown that reducing the supply voltage is the most direct means of reducing dissipated power and operating CMOS devices in the sub threshold region is considered to be the most energy-efficient solution for low-performance applications. The number of voltage domains within an integrated circuit is increasing to satisfy stringent power budgets. The increase in the number of voltage domains requires new techniques to generate these voltages close to the load circuitry [2] while occupying a small area. The power savings is greater when the voltage regulators are close to the load devices, and size is therefore the primary issue for point-of-load voltage regulation. Classical Power supplies occupy large on-chip area and are therefore not appropriate for Point-of-load power delivery. Several topologies are commonly used to generate on-chip dc voltages. These DC–DC voltage converters are generally used as on-chip power supplies in high performance integrated circuits. Conventional DC–DC converters can be grouped into three primary categories: switching, switched capacitor (SC), and linear DC–DC converters [3]. Buck converters, which are step-down switching DC–DC converters, are popular because of their high power efficiency. A second order inductor–capacitor (LC) passive filter[3] is commonly used in a buck converter. The passive LC components require significant on-chip area therefore, the passive components have generally been implemented off chip. As a consequence of placing these components off-chip, significant voltage drop and bounce are produced at the package level due to the parasitic resistance and inductance between the off-chip components of the voltage converter and the integrated circuit.

II. Related Works

Many techniques have been developed to reduce power dissipation in dc-dc converter. In this section, we briefly review some existing work related to the proposed technique.

Volkan Kursun, Siva G. Narendra, Vivek K. De, and Eby G. Friedman proposed an analysis of an on-chip buck converter is presented in this paper. A high switching frequency is the key design parameter that simultaneously permits monolithic integration and high efficiency. A model of the parasitic impedances of a buck converter is developed. A buck converter is a standard switching dc–dc converter circuit topology with high efficiency and good output voltage regulation characteristics. Buck converters are used to generate a regulated dc output supply voltage from a higher (possibly no regulated) dc input voltage. Buck converters are popular due to the high efficiency and good output voltage regulation

characteristics of these circuits. In single power-supply microprocessors, the primary power supply is typically an external (nonintegrated) buck converter.

The analytical expression for the total power consumption of a buck converter is effective in estimating the circuit efficiency characteristics. The buck converter efficiency as determined by simulation at the target design point is 86%, which only differs by 2.4% from the efficiency determined from the analytic expression.

Selc¸uk K¨ose and Eby G. Friedman proposed an area efficient fully monolithic hybrid voltage regulator. A hybrid voltage regulator module for an on-chip DC-DC voltage converter is proposed in this paper. The circuit is appropriate for point-of-load voltage regulation due to an ultra area efficient architecture. The proposed voltage regulator is a hybrid combination of a switching DC-DC voltage converter and a low-dropout regulator exploiting active circuitry rather than bulky passive devices within the filter structure. One method is to use decoupling capacitors to reduce the impedance of the power distribution network over a wide frequency range. Since the active devices switch at high frequencies, the decoupling capacitors require sufficient time to recharge before the next switching event. The efficacy of the decoupling capacitors depends upon the distance from the decoupling capacitor to the power supply. Both off-chip and on-chip DC-DC voltage converters are generally used to supply power to modern ICs. Conventional DC-DC converters can be grouped into three categories.

Switching, switched capacitor, and linear DC-DC converters. A pulse width modulator (PWM) generates a switching signal which drives tapered buffers which drives large NMOS and PMOS transistors. The proposed active filter-based DC-DC voltage converter has been designed in a 90 nm CMOS technology. The input switching signal frequency is 100 MHz A modified ring oscillator1 supplies the switching signal to the input. Since there is no need for large tapered buffers, the power dissipated by the ring oscillator and output buffers is relatively small. The proposed circuit can supply over 100 mA current while generating 0.9 volts from a 1.2 input voltage, exhibiting a high current efficiency of greater than 99%. The on-chip area is 0.026 mm2 which is 500 times smaller than a monolithic buck converter and four times smaller than an LDO. The proposed regulator provides a means for distributing multiple local power supplies across an integrated circuit while providing high current efficiency

Selc¸uk K¨ose and Eby G. Friedman, Simon Tam, Sally Pinzon and Bruce McDermott proposed active filters based on chip hybrid voltage converter are described in this paper. The area of the voltage converter is significantly less than the area of a conventional passive filter based DC-DC voltage converter or a low-dropout (LDO) regulator. Hence, the proposed circuit is appropriate for point-of-load voltage regulation for the noise sensitive portions of an integrated circuit. An area efficient voltage converter is required for the next generation of multi-voltage systems because these systems are highly sensitive to local power/ground (P/G) noise. To produce a voltage regulator appropriate for distributed point of- load voltage generation, the passive LC filter within a buck Converter is replaced with a more area efficient active filter. A switching voltage is generated at the input of the active filter and the converter with this filter structure produces the desired output voltage. The current supplied to the output node, however, does not originate from the input switching signal; rather, from the operational amplifier (Op Amp) output stage, similar to a linear voltage converter. This voltage converter is therefore a hybrid combination of a switching and linear DC-DC converter. In this paper, experimental results characterizing this promising hybrid voltage regulator topology is experimentally verified.

Design tradeoffs among area, maximum load current, and load regulation are evaluated with experimental results. The on-chip area of this hybrid regulator is 0.015 mm2 with a mature 110 nm CMOS technology, significantly smaller than state-of-the-art output capacitor less LDOs. the proposed circuit, the bulky LC filter in a conventional buck converter is replaced with an active filter structure and the tapered buffers are replaced with smaller buffers. The advantages and disadvantages of an active filter based, conventional switching, linear, and switched capacitor voltage converters are compared. The proposed circuit provides a means for distributing multiple local power supplies across an integrated circuit while maintaining high current efficiency and fast response time within a small area**.**

III. DC-DC Converter

The power supply voltage aggressively scales with each technology generation, making the delivery of a high quality supply voltage to noise sensitive circuit blocks highly challenging. The number of voltage domains within an integrated circuit is increasing to satisfy stringent power budgets. The increase in the number of voltage domains requires new techniques to generate these voltages close to the load circuitry while occupying a small area. The power savings is greater when the voltage regulators are close to the load devices (point-of-load voltage delivery), and size is therefore the primary issue for point-of-load voltage regulation. Classical power supplies occupy large on-chip area and are therefore not appropriate for point-of-load power delivery. Several topologies are commonly used to generate on-chip dc voltages. These DC–DC voltage converters are generally used as on-chip power supplies in high performance integrated circuits. Conventional DC–DC converters can be grouped into three primary categories: switching, switched capacitor (SC), and linear DC–DC converters.

A. DC-DC Converter with active filter

The existing technique of dc-dc converter with active filter consists the switching input signal generated at Node1 is filtered by the active filter structure, similar to a buck converter, and a dc voltage is generated at the output.

Two topologies are popular for implementing an integrated low pass active filter, i.e., multiple feedback and Sallen–Key. Multiple feedback low pass filters use capacitive and resistive components within the feedback path from the output to the input. A dc current path exists between the input and output nodes due to the resistive feedback, as shown in Figure 2. The dc current increases the power dissipated by the multiple feedback active filter. Multiple feedback active filters are therefore less suitable for an active filter-based on-chip voltage regulator. Alternatively, Sallen–Key low pass filters use only capacitive feedback. Hence, the static power dissipation of the Sallen–Key topology is significantly less than that in the multiple feedback topologies.

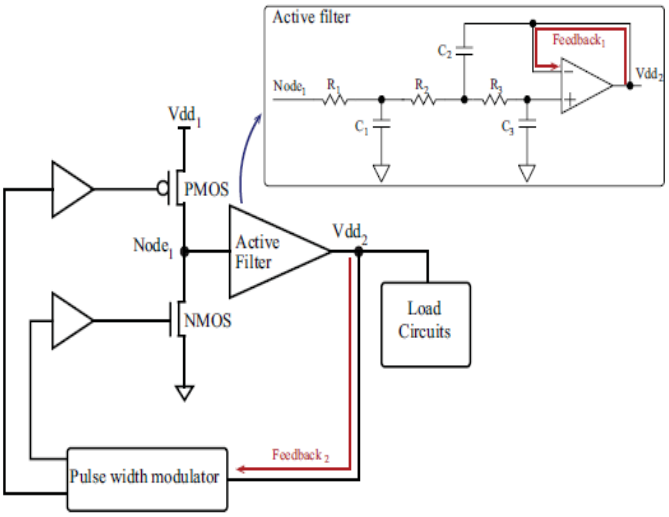

Fig. 1 DC-DC converter with active filter

The gain of the active filter can be increased by inserting resistive feedback between the non inverting input and output nodes, forming a dc current path between the output and ground. The performance of an active filter depends strongly on the Op Amp. The gain–bandwidth product of the Op Amp determines the bandwidth of the active filter. Most of the power loss takes place within the Op Amp structure, since the current provided to the output load is supplied by the Op Amp output stage. Hence, the Op Amp needs to provide tens of milliamps of current to the load devices while maintaining sufficient performance to reliably operate the active filter.

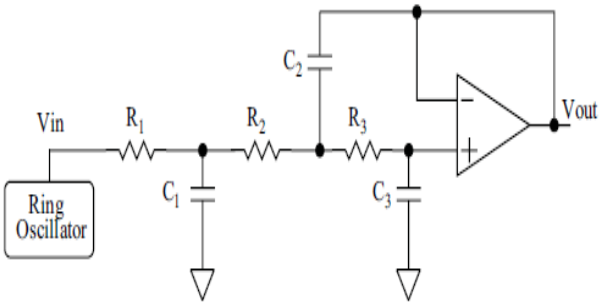

Fig. 2 Active low pass Sallen–Key filter circuit.

A three stage classical differential-input single-ended CMOS Op Amp structure is utilized in the proposed regulator, as shown in Figure 3.

B. Ring oscillator design

A ring oscillator only requires power to operate; above a certain threshold voltage, oscillations begin spontaneously. To increase the frequency of scillation, two methods are commonly used. Firstly, the applied voltage may be increased; this increases both the frequency of the oscillation and the current consumed. The maximum permissible voltage applied to the circuits limits the speed of a given oscillator. Secondly, making the ring from a smaller number of inverters results in a higher frequency of oscillation given certain power consumption.

Active filter structures contain no passive inductors. The filtering function uses capacitors, resistors, and an active circuit (i.e., the Op Amp). Certain design considerations should be considered when utilizing an active filter as a voltage regulator since the appropriate active filter topology depends upon the application.

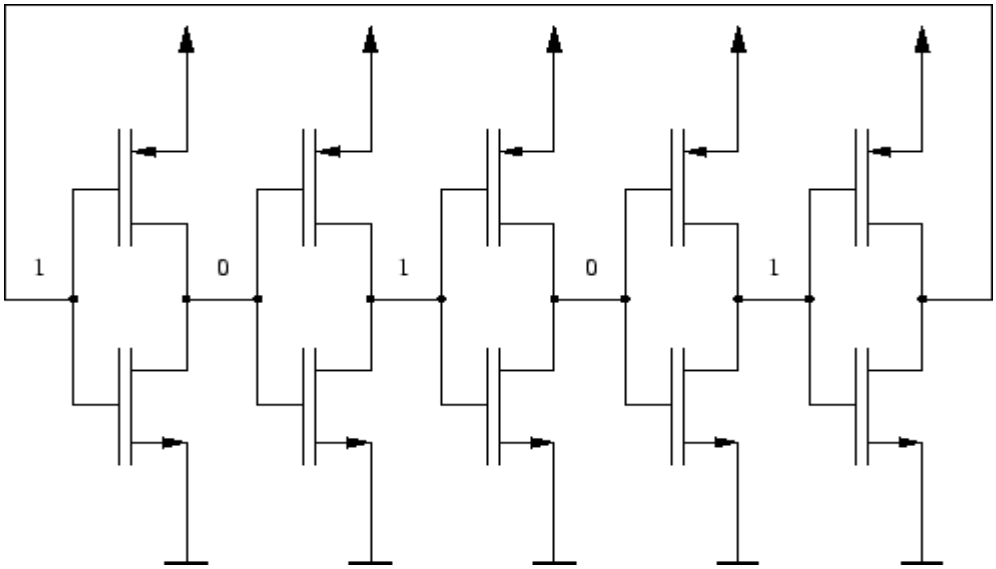

Fig.3 Ring Oscillator

Dynamic leakage control circuits for use with graphics processor circuitry are described. The dynamic leakage control circuit selectively enables back biasing of the transistors comprising the graphics processor circuits during particular modes of operation. Microprocessor circuits typically operate in two primary operating states, active mode and standby mode. In active mode, the circuits are executing processes or tasks, and are usually running at the specified operating frequency of the circuit. During active mode, most of the transistor gates are switching and relatively high operating frequencies are required.

The proposed ring oscillator circuit show in fig 4. The power consumed in transistor circuits is a function of both switching power and leakage power. Even when a circuit is in standby mode, potentially significant amounts of power can be consumed due to power leakage in the transistors.

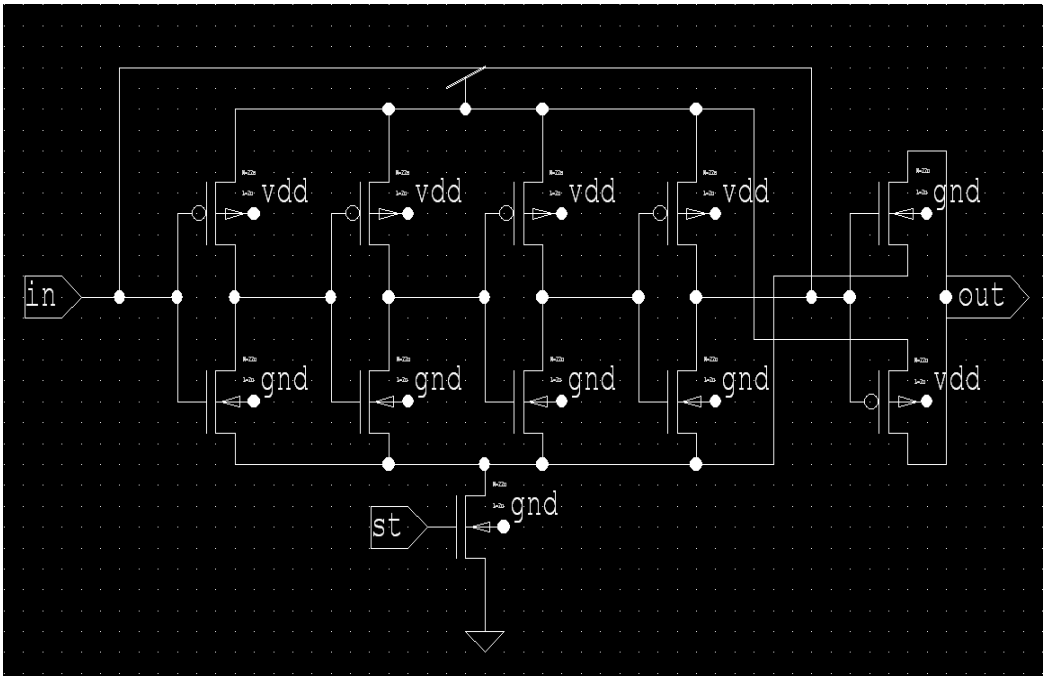

Fig.4 Proposed Ring Oscillator

IV. Evaluation and discussion

In this section, we evaluate the proposed technique by comparing energy savings with existing op-amp design techniques. This chapter deals with simulation results and discussions of the DC-DC CONVERTER. The software tool used is TANNER. The output of low power using schematic edit(S-EDIT) is taken. The power analysis in DC-DC

CONVERTER is obtained with the help of TANNER tool. The dc-dc converter architecture discussed in this project uses newly modified op-amp logic in order to reduce the power consumption. The simulated results using TANNER software is given for the proposed op-amp design.

Then the synthesis report which shows the total power consumption is presented next. Finally a comparison is made with conventional op-amp design.

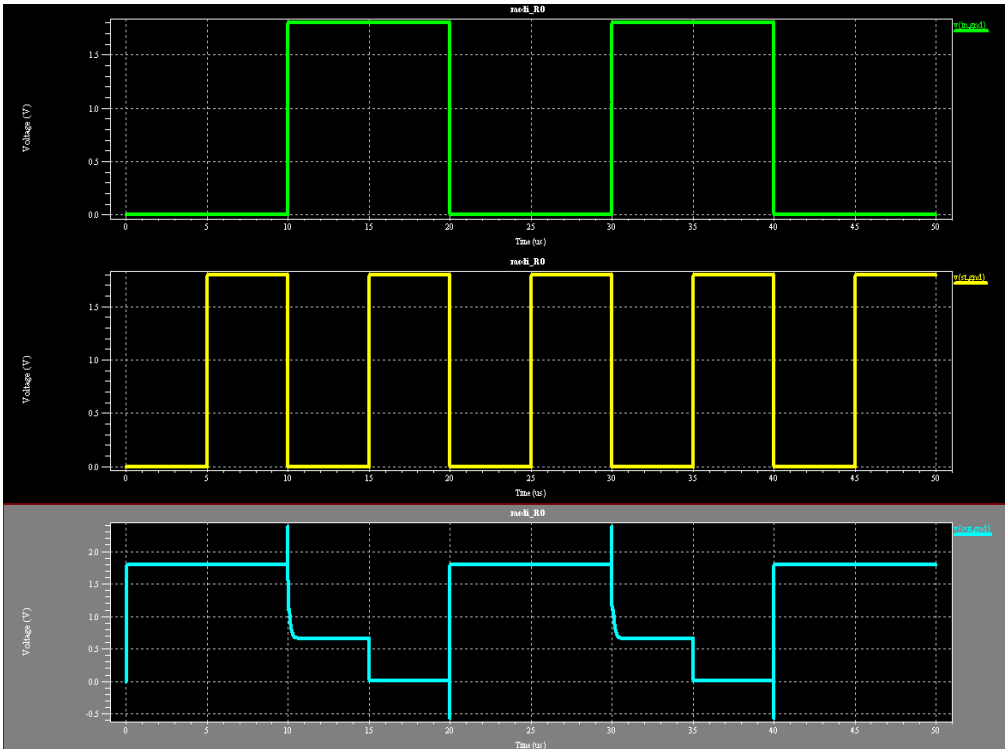

Fig.5 Output Wave Form Of Ring Oscillator

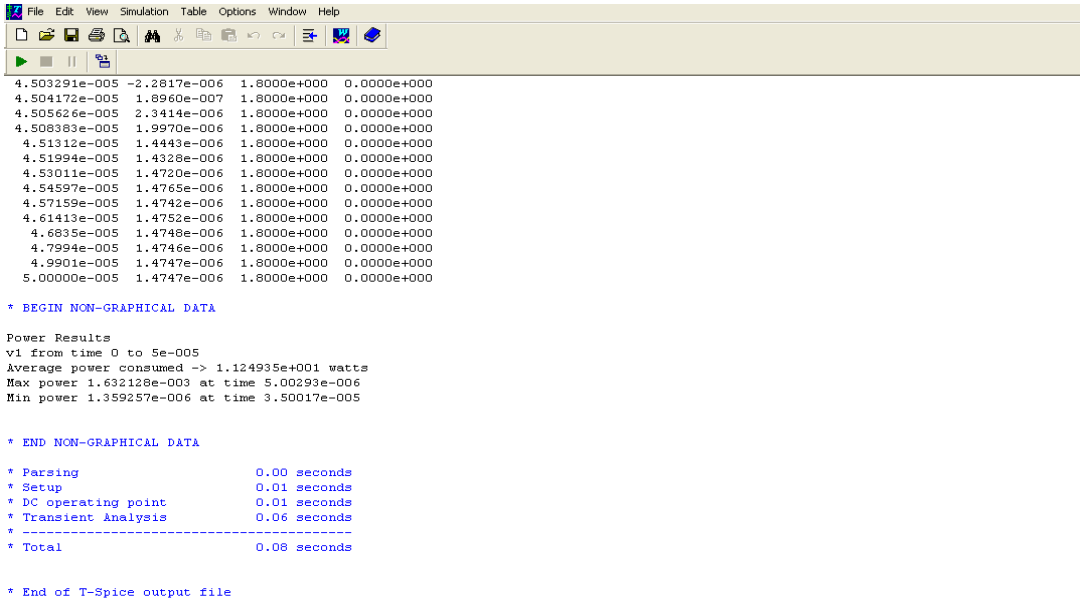

Fig.6 Output power of ring oscillator

V. Conclusions

From the power analysis it shows that the total power consumption by the proposed active filter is reduced. Maximum power in ring oscillator is 0.00163(w) were as in conventional design 0.1811(w), so the proposed system has reduced 75% power consumption than conventional technique. The proposed technique achieves 50% energy saving with area reduced.

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