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Design and Analysis of Multipliers Using Energy Recovery Adiabatic Logics

Punitha.S[1],
[1]Assistant Prof., Department of ECE,
SVS College of Engineering, India

Deebika.R[2]
Department of ECE
SVS College of Engineering, India

Karunambiga.R[3]
Department of ECE,
SVS College of Engineering, India

Priya.K[4]
Department of ECE,
SVS College of Engineering, India

Abstract –

In today's world low power issues have become a major important factor in modern VLSI design. In fact, Low Power VLSI chips have emerged as highly in demand for designing any subsystem. Low power circuit is realized using both hardware and software approach. [12] The limited power capacity of the portable system has lead designers to more power aware designs. Energy efficient circuits are required because of the increasingly stringent demands for battery space and weight in portable multimedia devices, particularly in digital multipliers which are basic building blocks of digital signal processors. Besides adders, digital multipliers are the most critical arithmetic functional unit in many DSP applications such as in filters, Fourier transform and discrete cosine transform and in multiplier accumulate unit. In this paper we are going to design multipliers using ECRL & PFAL logics and the performance of these energy recovery adiabatic logics are compared in terms of power dissipation, energy consumption & operating frequencies. The multipliers are designed using adder or compressor and the power results are obtained using Tanner EDA 13.0 tool.

Keywords – Adiabatic logic, Multipliers, ECRL logic, PFAL logic, Performance Comparison.

I. INTRODUCTION

As the transistor count per chip increases rapidly in the system-on-chip (SoC) era, significant reduction in power overhead in dynamic switching and leakage is of particular importance. Adiabatic logic style has emerged as a promising approach to achieve ultra-low power without sacrificing noise immunity and driving ability. Adiabatic circuits achieve low energy dissipation by restricting the current flow across devices with low voltage drop and by recycling the energy stored on their load capacitance by using a time varying AC supply voltage.

Reversible logic is used to overcome the power challenge of the traditional digital integrated circuits potentially benefits from the associated energy recovery enabled by the reversible computation principles. Standard Complementary Metal Oxide Semiconductor (CMOS) technology does not recover signal energy, which leads to considerable energy waste and heat dissipation, limiting the attainable device densities and operating frequencies, and thereby, also the available computing power. Adiabatically charged logic recovers part of the signal energy, and if the circuits are slowed down, asymptotically nearly all of the energy can be recovered. The cost of asymptotically adiabatic logic is usually high in circuit area, complexity, or timing. Either reversible logic gates or timing-based logical reversibility is required.

All the simulation are done by Tanner EDA in 180nm technology and results are compared with these imperative adiabatic logic styles including static CMOS also. Extensive experiments are done to ensure more accurate performance evaluation among all the reported logics and also to show the feasibility for designing of adiabatic circuitry that functions properly at relatively high power clock frequency. The rest of the paper is organized as follows. Rudimentary principles of transistor based adiabatic switching with a brief review of some imperative adiabatic logics are presented in section II. Section III compares the energy recovery logics. Experimental results and comparison of performance of imperative energy recovery logics are also detailed in section IV. Finally conclusions are given in section V.

II. TRANSISTOR BASED ADIABATIC LOGICS

The term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. In this the main design changes are focused in power clock which plays a vital role in the principle of operation.

Adiabatic circuits attempt to conserve charge by following three key rules:

1. Never turn on the transistor when there is a voltage potential between the source & drain (V_{ds}>0).
2. Never turn off a transistor when current is flowing through it (I_{ds}-0)
3. Never pass current through a diode.

When the 3 conditions are satisfied with regard to the inputs, in all the 4 phases of power clock, recovery phase will restore the energy to power clock, resulting considerable energy saving. Thus the adiabatic logic circuits operate without loss or gain of electric charge.

III. SIGNAL ENERGY RECOVERY LOGICS

The energy-efficiency of any integrated circuit technology is closely related to the method of signal representation and the associated signal energy, which has to overcome the thermal noise floor by a significant margin. In standard static CMOS, every switching event leads potentially to the dissipation of all the signal energy related to a certain circuit node. Most of this loss can be avoided by utilizing adiabatic charging principles, which can be fully implemented only by logically reversible circuits. There are two types' namely positive feedback adiabatic logic (PFAL) and efficient charge-recovery logic (ECRL).

Efficient Charge Recovery Logic (ECRL) and Positive Feedback Adiabatic Logic (PFAL) are partially adiabatic techniques. ECRL is based around a pair of cross-coupled PMOS transistors. Their source terminals are connected to the power-clock, and the gate of each one is connected to the drain of the other. These nodes form the complementary output signals. The function is evaluated by a series of pull-down NMOS devices [3]. The basic structure of ECRL circuits is shown in figure 1. The core of the PFAL circuits is a latch made by the two PMOS and two NMOS, that avoid a logic level degradation on the output nodes " out" and " /out" . The two n- trees realize the logic functions. This logic family also generates both positive and negative outputs. Figure 2 shows the PFAL basic structure.

3.1 POSITIVE FEEDBACK ADIABATIC LOGIC

Adiabatic logic family generates both positive and negative outputs. The two major differences with respect to ECRL are that the latch is made by two p MOSFETs and two n MOSFETs, rather than by only two p MOSFETs as in ECRL, and that the functional blocks are in parallel with the transmission p MOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged. The ratio between the energy needed in a cycle and the dissipated one can be seen in figure 6. During the recovery phase, the loaded capacitance gives back energy to the power supply and the supplied energy decreases. The sum and carry circuit of PFAL is given in fig: 1 & 2.

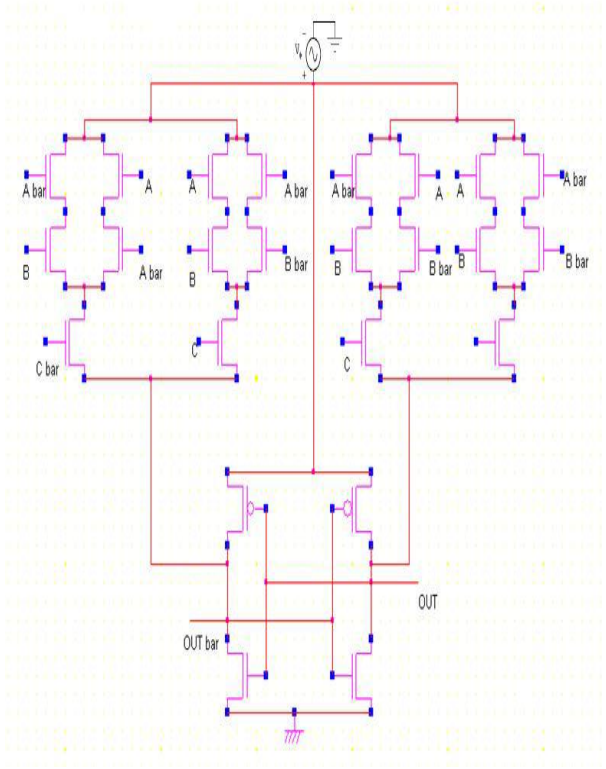

Fig 1: PFAL sum circuit

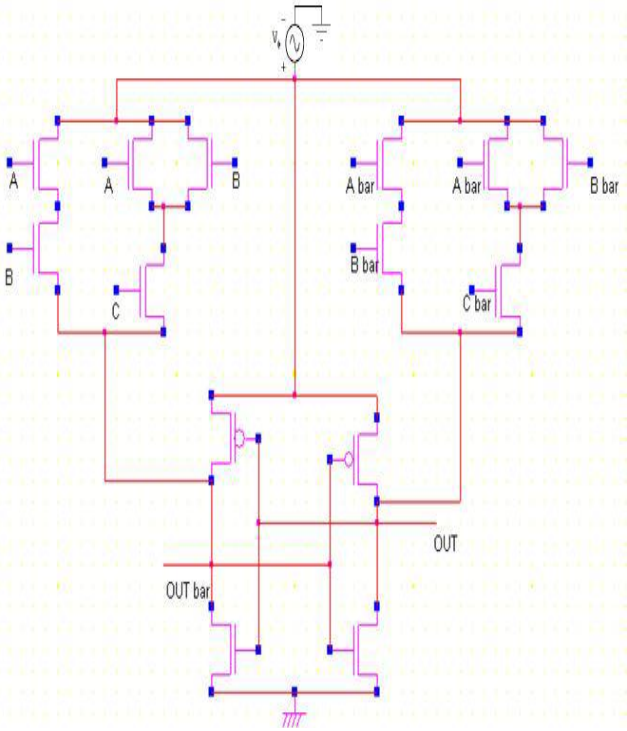

fig 2: PFAL carry circuit

3.2 EFFICIENT CHARGE-RECOVERY LOGIC

ECRL uses cross- coupled PMOS transistors. It has the structure similar to Cascade Voltage Switch Logic (CVSL) with differential signaling. An AC power supply power is used for ECRL gates, so as to recover and reuse the supplied energy. Both out and /out are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. A more detailed description of ECRL can be found in. Full output swing is obtained because of the cross-coupled PMOS transistors in both recharge and recover phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the recharge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. The sum circuit is given in fig:3 and carry circuit in fig:4.

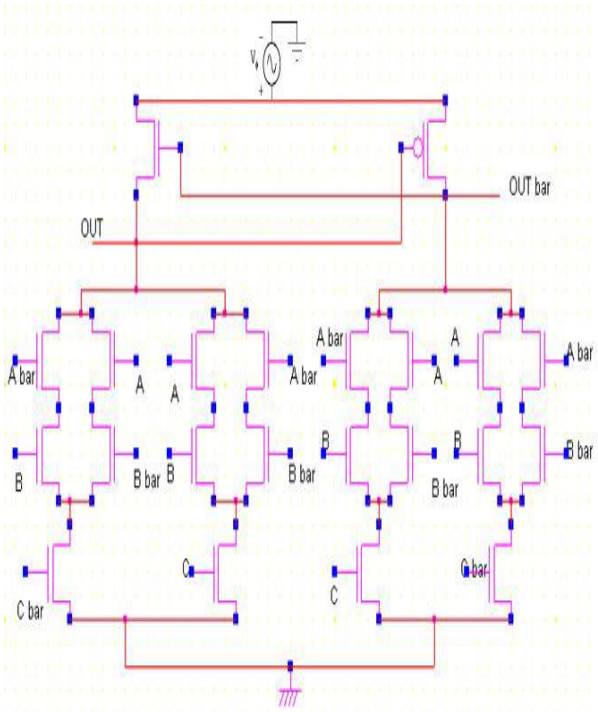

Fig 3: ECRL sum circuit

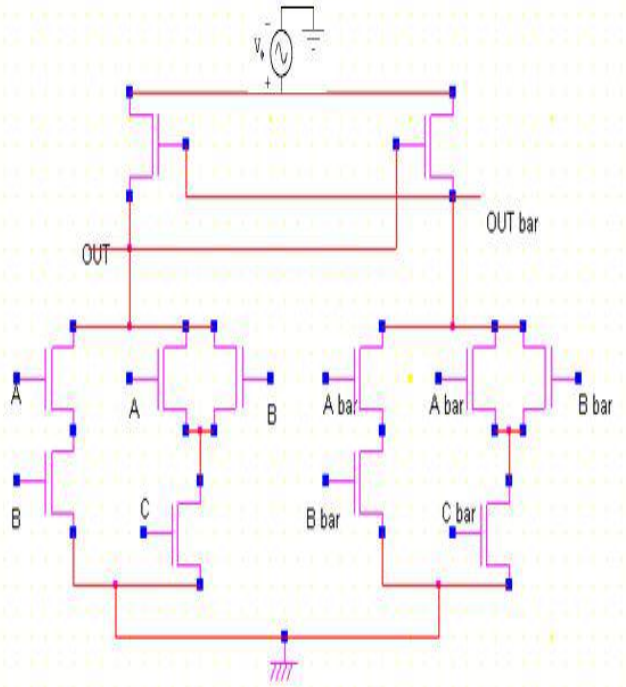

fig 4: ECRL carry circuit

IV. MULTIPLIER DESIGN

The designed 8×8 multiplier unit is based on a standard combinatorial structure laid out manually using CMOS transistors on an 180nm technology node. The significant modifications are related to the static operating voltage and ground networks, which have been replaced with dynamic power-clock signals. The n-type transistors have a W/L ratio of 6µm / 2µm with a threshold voltage of 0.7V, while the p-type transistors have a W/L ratio of 12 µm / 2µm with a threshold voltage of -0.5V. The gate oxide thickness is 20nm.

4.1 LOGICAL STRUCTURE AND IMPLEMENTATION:

The combinatorial structure of the standard multiplier unit is inherently logically Irreversible, composing of standard CMOS logic gates and not utilizing any registers [9]. The unit takes as input two 8-bit words A = (A7, A6, A5, A4, A3, A2, A1, A0) and B = (B7, B6, B5, B4, B3, B2, B1, B0) and produces the 16-bit output word F = (F15, F0). The unsigned binary multiplication is defined if Fig. 3(a), while the grouping used for the addition of the summands AiBj in the implementation is depicted in Fig. 3(b). The structure of multipliers designed using ECRL and PFAL logic is shown in fig. (1)

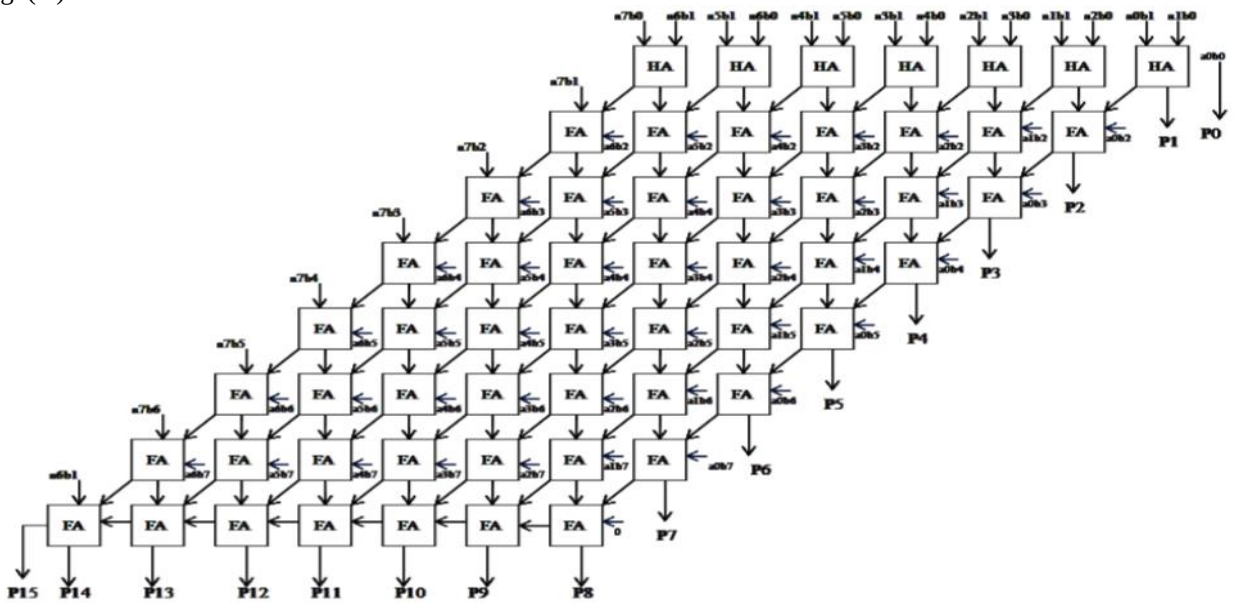

Fig 5: Architecture of standard 8×8 multiplier

4.2 IMPLEMENTATION OF MULTIPLIER USING ECRL:

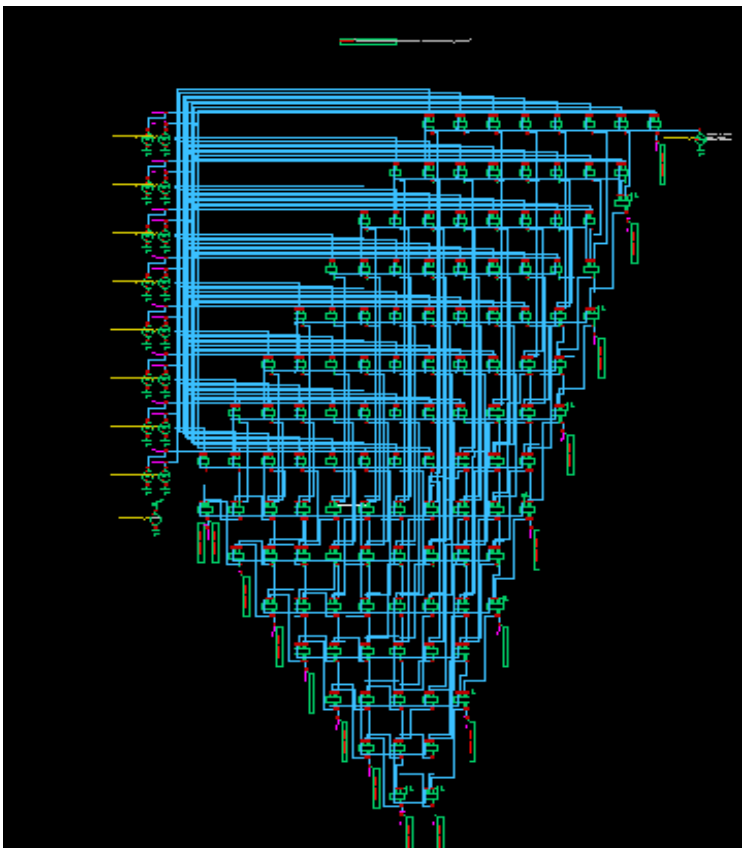

Fig 6: multiplier circuit using ECRL

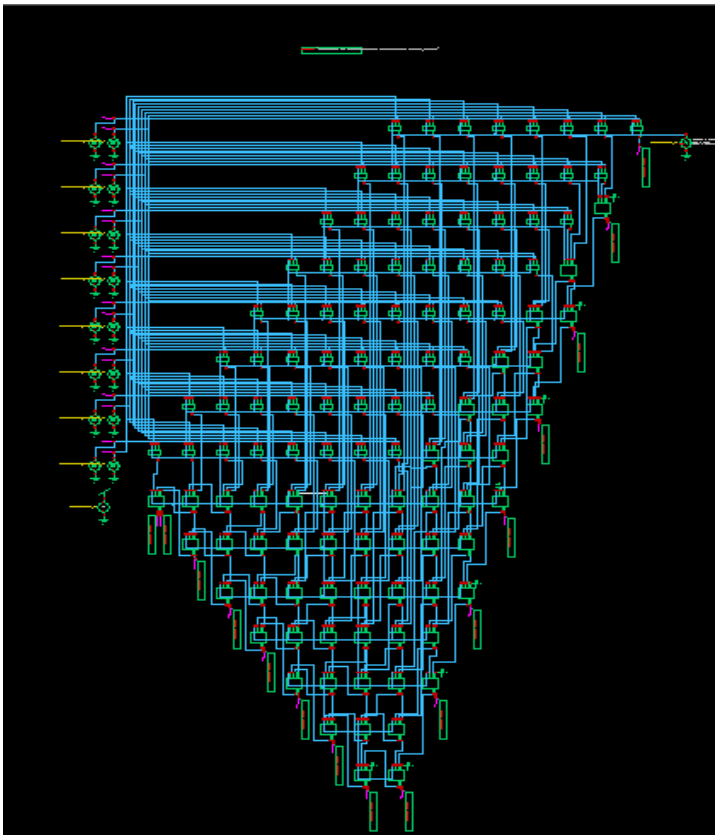

Fig 7: Multiplier circuit using PFAL

V. SIMULATION RESULTS

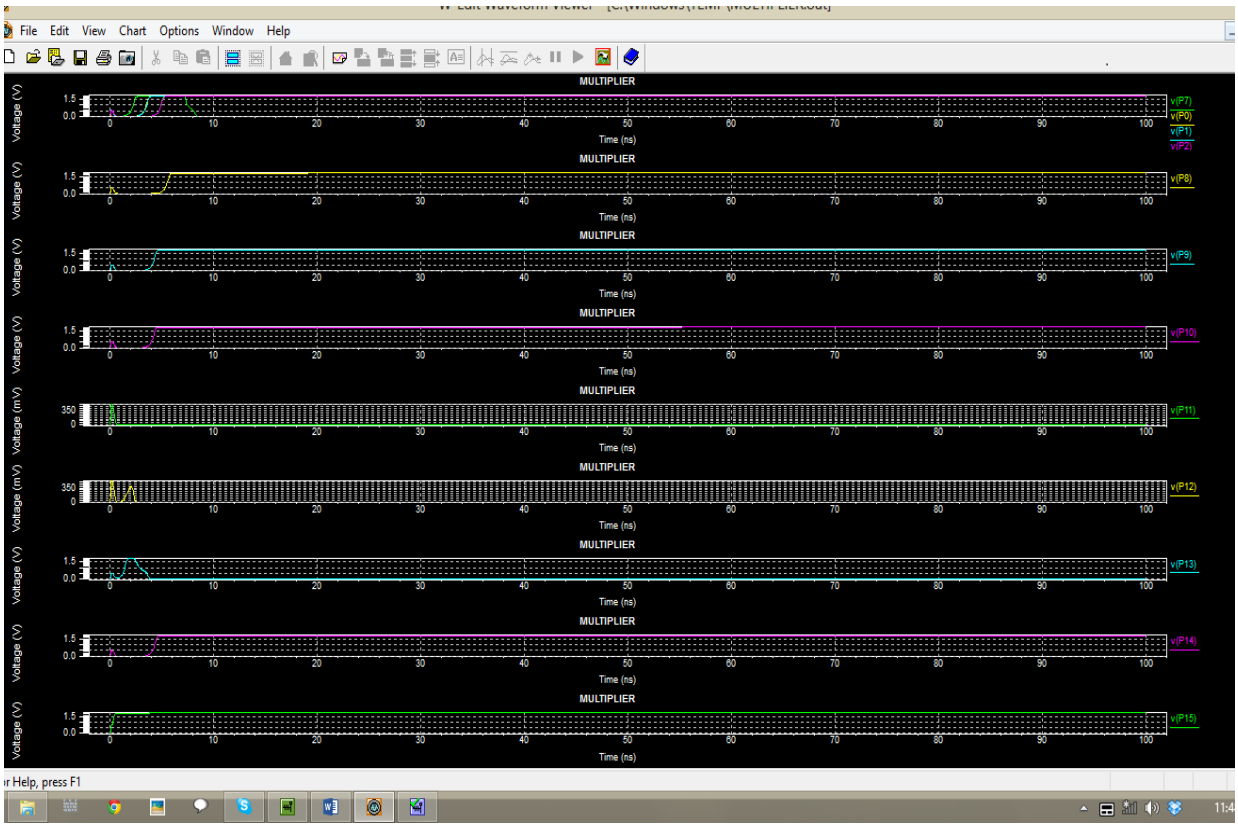

Fig 8: multiplier output using ECRL

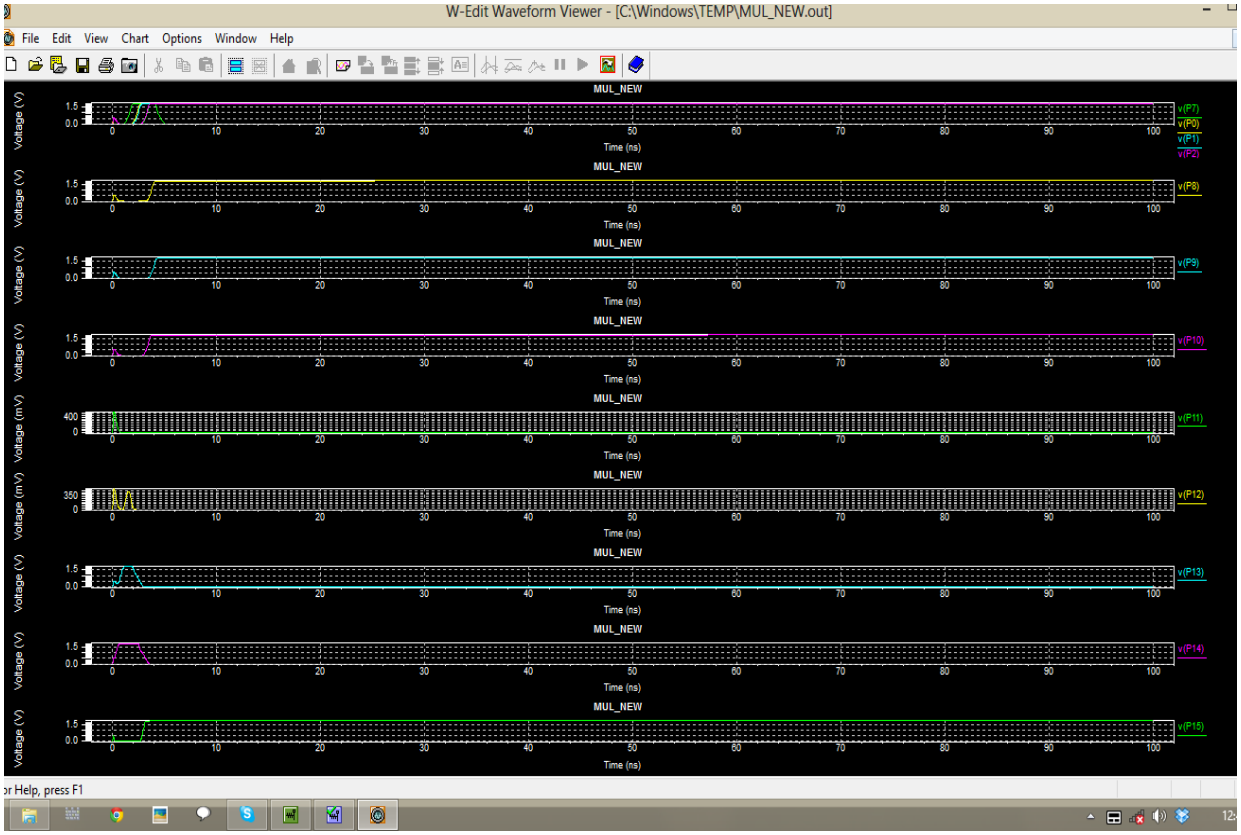

Fig 9: multiplier output using PFAL

The figure above shows the simulated output waveform of ECRL and PFAL. There are 16 output waveform shown. The outputs are determine in form of binary 1's and 0's.

POWER RESULTS:

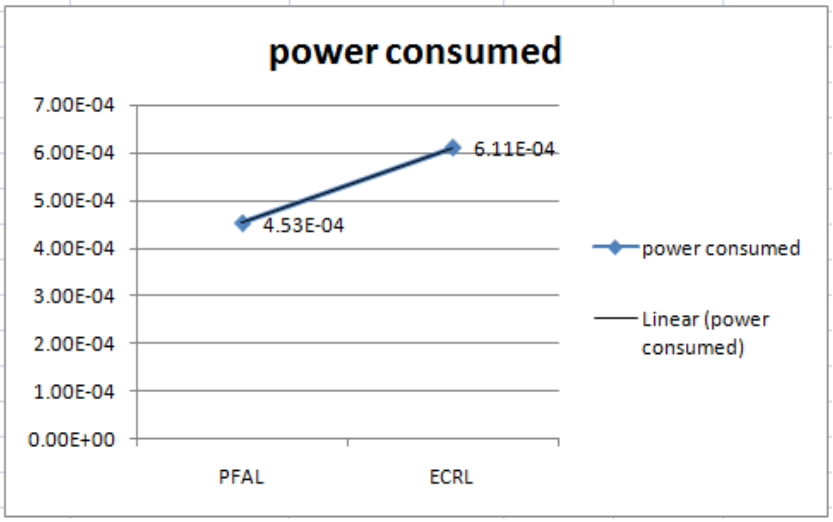

Fig 9: power results of ECRL & PFAL

VI. CONCLUSION

This paper proposes energy efficient adiabatic logic for digital circuits. The results were simulated using TANNER EDA and comparison has been done for different parameters of multiplier in different adiabatic logic styles. The results show that the proposed adiabatic logic has less power dissipation compared to conventional CMOS design and it also uses less power supply. These advantages made this logic more convenient for energy efficient digital applications.

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