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Fault Simulation Using Parallel Fault Simulation with Advanced Fault Injection Technique

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Abstract:

The procedure for accelerating fault simulation in VLSI testing is to reduce the fault simulation time. The parallel simulation methodology in large circuits significantly reduces the fault simulation time. Fault simulation can be parallelized either by portioning set of faults or set of vectors or both. The fault tolerance and reliability of a circuit cannot be continuously evaluated with a bench mark circuit .The remedy for this problem is, the effect of fault is created in simulation model. In this generally accepted solution can be implemented by VHDL code modification technique, either saboteurs or by mutants. This paper deals with the component replacing method, mutants method. Then fault verification is done by test vector that already stored in memory location of RAM.

Keywords— ***Fault Tolerance ,Mutants, Saboteurs, Fault verification, Fault injection, Test vectors***

I. INTRODUCTION

.The present day, fault tolerance is important to maintain the system functioning with least amount of time and impact to the operation application and infrastructure objects. The acceleration of fault simulation a technique for making efficient fault tolerance. The fault verification can be done by two methods .That are simulation on PC and another is simulation on actual hardware. This paper deals with simulation PC ,that is software simulation. VHDL coding is used for simulation on PC technique. The parallel fault simulation methodology is used for testing the system. This approach will reduce the fault simulation time. There by increases reliability and fault tolerance of the system. A good circuit and fixed number of faulty circuits are simultaneously simulated in parallel methodology. The circuit partitioning can be done by two methods parallel to sensitization path and vertical to sensitization path. This proposed method of circuit partitioning will increase the system efficiency and save hardware resources

Checking of fault tolerance of system under test through a benchmark circuit is not much easy. The continues evaluation is time consuming ,so solution for this problem is inserting the effect of fault in circuit under test . By this fault injection mechanism the simulation time can be reduced to a great extent. Fault injection in the VLSI testing by VHDL code modification techniques ,that are saboteurs and mutants .The first one is based on adding extra components to the simulation model. These inserted components are specifically for fault injection, and are called saboteurs. The second method deals with modifying components in the simulation model, generating altered description of components called mutants. Mutants method of replacing component is used in simulation model specified in this paper. When inactive it works like original component ,but when activated it behaves like faulty component .Fault verification is based on a test vector that is already stored in RAM memory .The RAM memory will contain the output of fault free circuit ,and at simulation time the circuit under test is compared with stored output in RAM memory. This comparison will give a result that if the circuit is faulty circuit or fault free circuit. If it is detected as faulty circuit ,then further comparison is need for finding where the fault is obtained. For this purpose we are comparing the output of faulty circuit with fault injected circuit output ,that also stored in RAM memory.

Objective

- Fault simulation speed increased by parallel partitioning method of the simulated system
- Fault injection for creating effect of fault in the system
  - Fault injection is done by mutants method that is each component in the circuit is replaced by another components for finding possible errors that may appear in the system
  - Fault injection will improve overall system performance , efficiency and also system reliability

II. OVER VIEW

The system designed and implemented for the purpose of improved performance in fault tolerance ,efficiency and reliability. The fault simulation of system under test is done on PC. The fault verification ,that is detection of error where it is occurred and causes of errors. The fault detection and verification become more easier and reliable by fault injection method .The possible error combinations are introduced in fault free circuit for getting effect of fault. The fault injected system outputs are stored in corresponding memory location for further comparison and verification. The injected fault will helpful for finding faulty areas on scan chain, and that will lead to correcting the circuit by replacing the circuit components on basis of detected error.

III. SYSTEM DESIGN AND IMPLIMENTATION

Over all system contain following implementation methods

- Simulation On PC
- Parallel simulation
- Fault injection
- Fault verification

A. Simulation on PC

For fault verification method basically done by two methods that is simulation on actual hardware or simulation pc. The simulation on actual hardware is very effective ,fast, and work in full speed but its very costly approach. Here we deals with simulation on PC method .Hardware description language, VHDL based coding is used for simulation on PC method .but some draw backs for this method it needs lot of algorithm , uses multi threading or multi processors and its very time consuming

B. Parallel Simulation

We know that the system that specified in this paper ,that is circuit for simulation is partitioned .The partition of circuit is based mainly on two active kinds of methods parallel to sensitization path and vertical to sensitization path. Circuit partitioning is based on some basic concepts and methods .That is starting with separation of each primary output ,then trace the circuit from primary output to input. The fan out of each sub circuit is not considered independently, the circuit partitioning should be satisfy above conditions. Vertical to the sensitization path technique is the basis of this paper. Figure 1 shows the vertical to sensitization path division. This is more efficient compared to parallel to sensitization path , because it needs only half of clock cycles that required for parallel sensitization [2]path, that is it two times faster than first method. We are using scan chains ,it scan along the chain and detect the faults along the sensitization path.

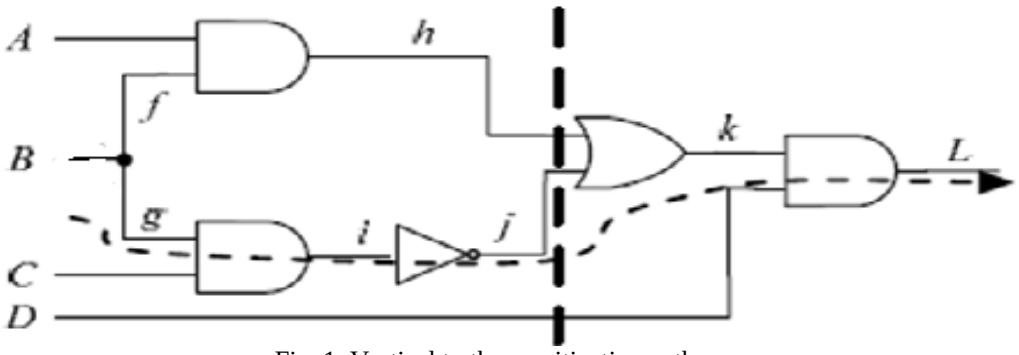

Fig. 1 Vertical to the sensitization path

C. Fault Injection

A major problem in the development of fault-tolerant systems is the accurate determination of the dependability properties of the system. Unlike performance, which can be evaluated through the use of benchmark programs, the degree of fault tolerance and reliability of a system cannot be evaluated in such a manner, since we do not often have the luxury of allowing systems to run for many years to see their behavior under fault effects. The generally accepted solution to this problem is to inject the effects of faults in a simulation model or a prototype implementation, and to observe the behavior of the system under the injected faults. Fault injection in a simulation is very flexible but far too time consuming. On the other hand, it is much more difficult to inject accurate faults into a prototype, but the effects of faults on operational code can be readily observed. Mainly two methods of Fault injection used in VLSI testing ,that are

- Saboteurs
- Mutants

1) Saboteurs

In this method we are adding a special VHDL component to the simulation model. This process is for altering the timing characteristics ,values original signal. The fault injected circuit is added with simulation model, it is known as saboteurs[1] .Here the extra VHDL components are added between the input and output ports are for the purpose of injection of fault.

2) *Mutant*

The paper deals with Mutants[1] method of fault injection, here component which replace another component. when inactive ,it works like a original component otherwise it behaves like a faulty circuit. There are eight fault models which

have a good correspondence with gate level faults . They can be classified in two groups that are fault in control flow and fault in data flow.

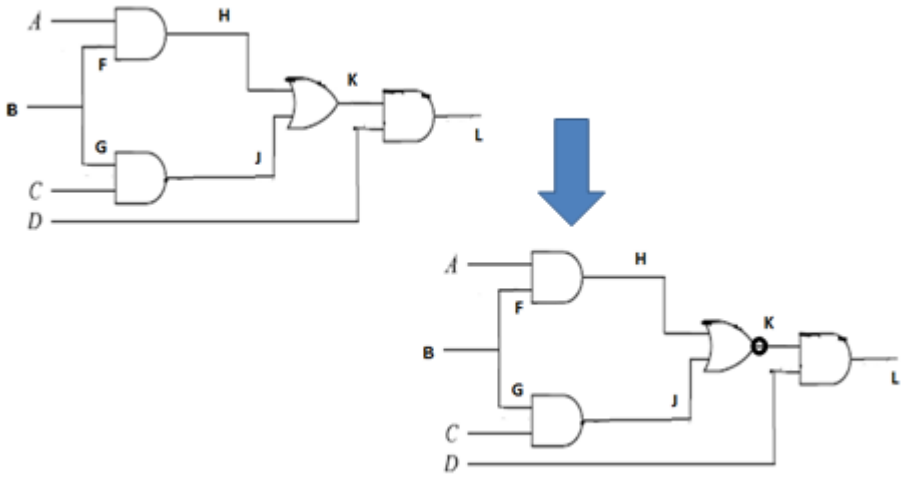

Fig. 2 Mutants method

D. Fault Verification

A fault verification apparatus performs a logic simulation of a circuit having a normal delay and a logic simulation of a circuit in which delay is intentionally changed for a node and compares the simulation results at a specific time and checks whether or not a test pattern can detect a fault due to a delay abnormality. The apparatus performs the logic simulation by applying the test pattern to the normal circuit and a variety of fault types and compares the expected values obtained from the results of the respective logic simulations and verifies whether or not the test pattern can detect the delay fault by whether or not the expected values are different from each other at a specific comparison point.

IV. WORKING OF THE SYSTEM

Working of simulation model can be explained as follows

- Storing of good data/ fault injected data
- Checking if the circuits are faulty or not
- Testing with test vectors

A. Storing Of Good Data/ Fault Injected Data

The first and second step that deals with storing of data in RAM. In first step the output corresponding to fault free circuit is stored in corresponding memory location of RAM. Storing of fault free data to the good RAM location. In second step the faulty circuits output is stored into B-RAM memory location.

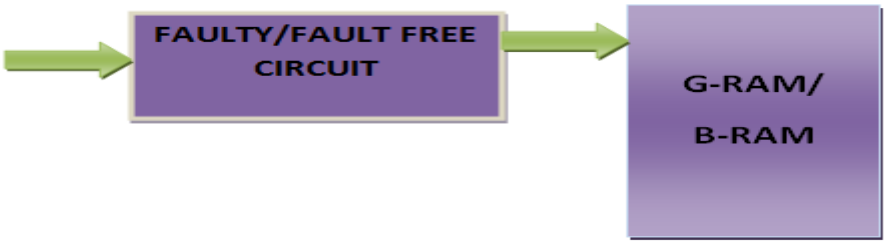

Fig.3 Storing of good data/ fault injected data

B. Checking if the circuits are faulty or not

The third step the output that reads from G-RAM is compared with the circuit under test output .If comparison result is positive then the circuit under test is fault free and can be used for further use. Otherwise there is a fault in the circuit and then circuit fault detection and error correction is required.

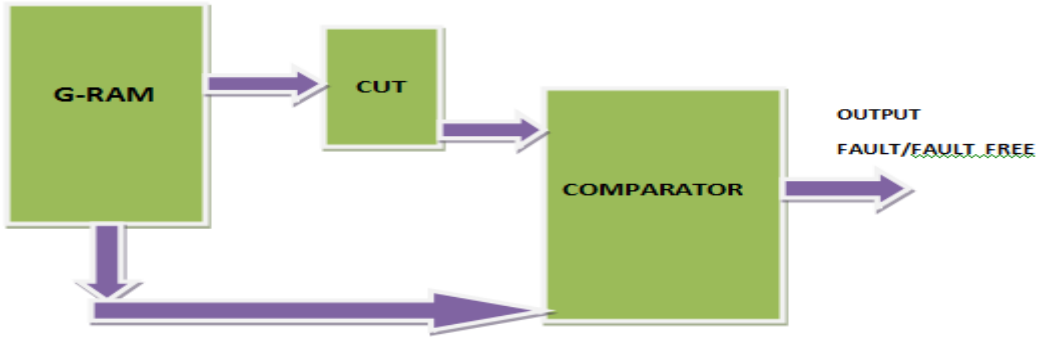

Fig .4 Checking if the circuits are faulty or not

C. Testing with test vectors

If it is detected that there is a fault in the simulated circuit then the comparison is taken place between the faulty output .if the result is positive then we can make an assumption that the error is occurred in the fault injected portion. Otherwise the fault is any other portion of circuit ,and we must find the faulty area

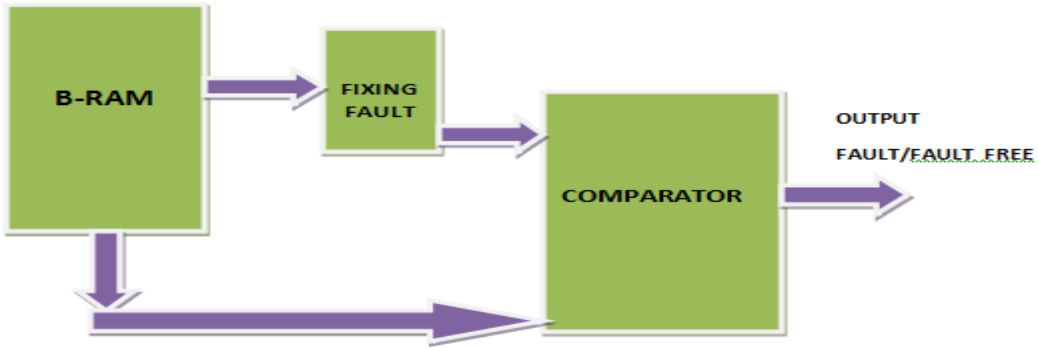

Fig.5 Testing with test vectors

V. Simulation Results

Simulation result obtained from the Simulation is given below. Modelsim is used for simulation,vertion Modelsim SE 6.3f is used.

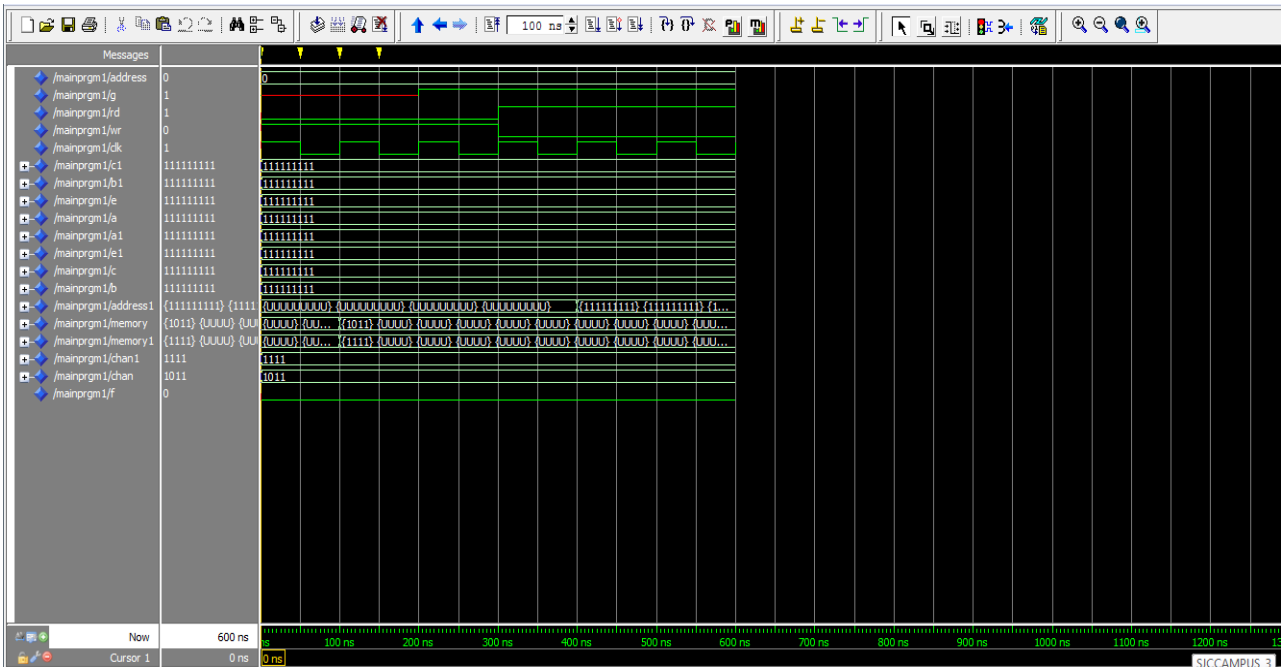

Fig.6Simulation result

VI. CONCLUSION

Fault tolerance and fault injection become more relevant in present day VLSI system simulation and testing. Through this paper trying to introduce a efficient mechanism for fault tolerance . Parallel simulation methodology is used for increasing fault simulation time. By fault injection and fault verification methods are used for error correction and error detection.

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